

14B24

Variant: [01] - Sample Production

11/03/2025
V2

RELEASED

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DESIGN CONSIDERATIONS

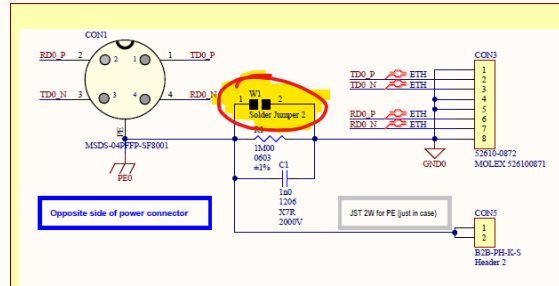
DESIGN NOTE:
Example text for informational
design notes .

DESIGN NOTE:
Example text for critical
design notes.

DESIGN NOTE:
Example text for cautionary
design notes.

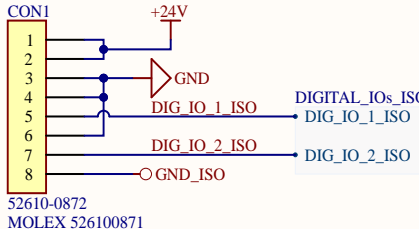
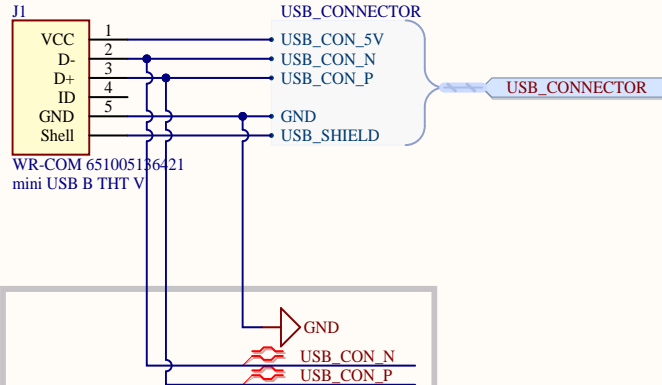
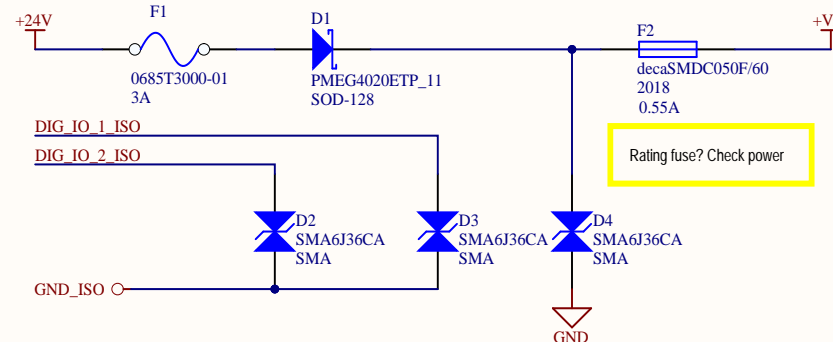
LAYOUT NOTE:
Example text for critical
layout guidelines.

See ../doc subfolder for full system architecture

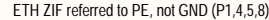


Title: 14B24		Kronotech Srl Via Adriatica, 284 33030 - Basaldella (UD) Italy
Size: A3	Revision: V2	
Date: 11/03/2025	Sheet 2 of 15	

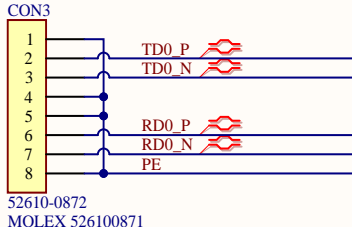
CONNECTORS


$$\begin{aligned} 6V \cdot 2A / 0.9 / (24-6)V &= 0.75A @ 18V I_{max} \\ 6V \cdot 2A / 0.9 / (24+6)V &= 0.45A @ 30V I_{min} \\ 6V \cdot 2A / 0.9 / (24)V &= 0.55A @ 24V I_{typ} \end{aligned}$$


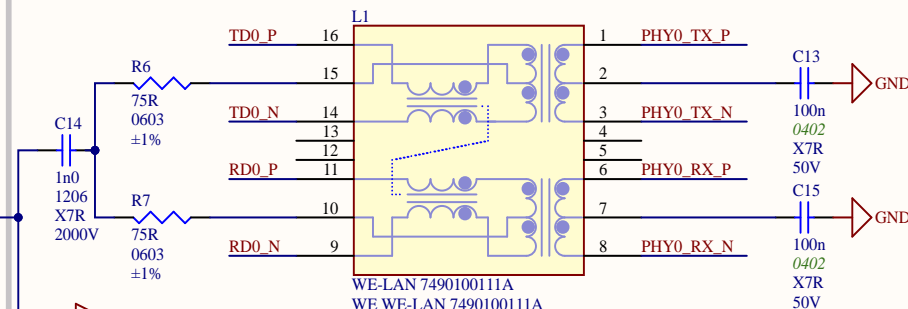
CON2 (ZIF to USB PCB): removed.



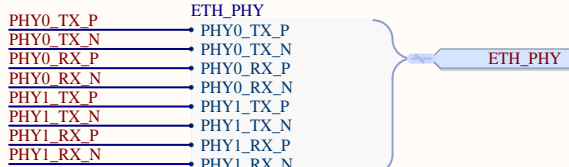
ZIF 8W ETH PHY0 to ETH connector board



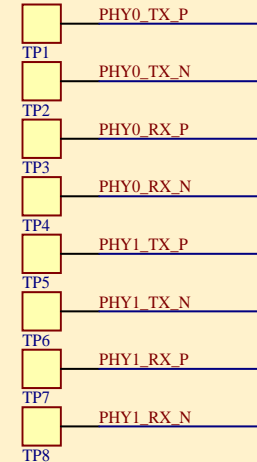
52610-0872
MOLEX 526100871



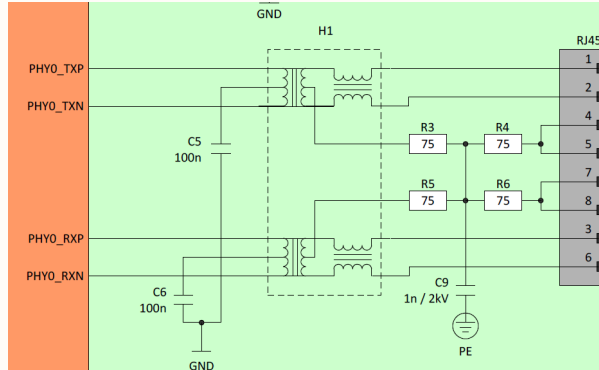
NO VIAS or TRACES UNDER the IC



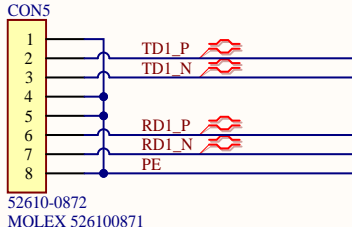
TEST POINTS ETH PHY



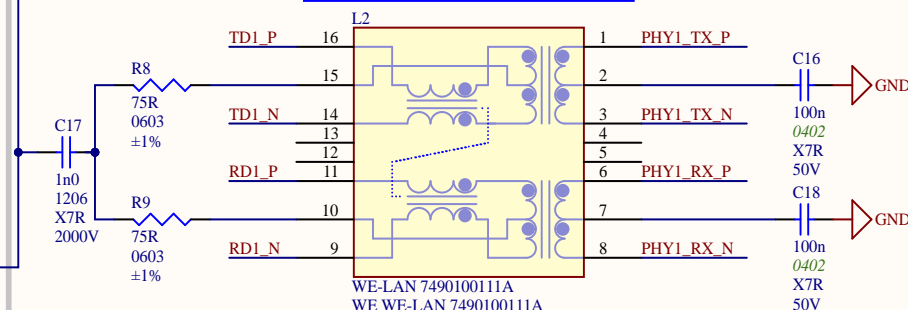
TPs on TOP
paired and grouped, but limit PHY impedance degradation



ZIF 8W ETH PHY1 to ETH connector board

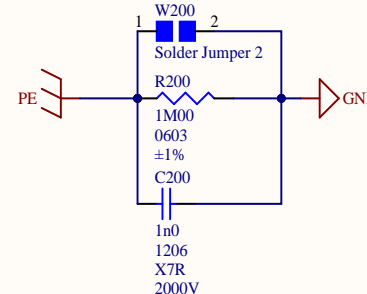
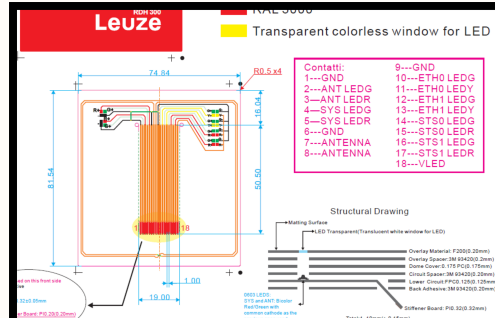
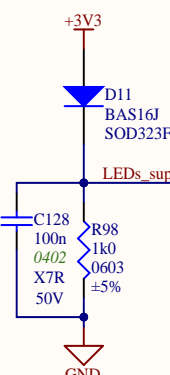
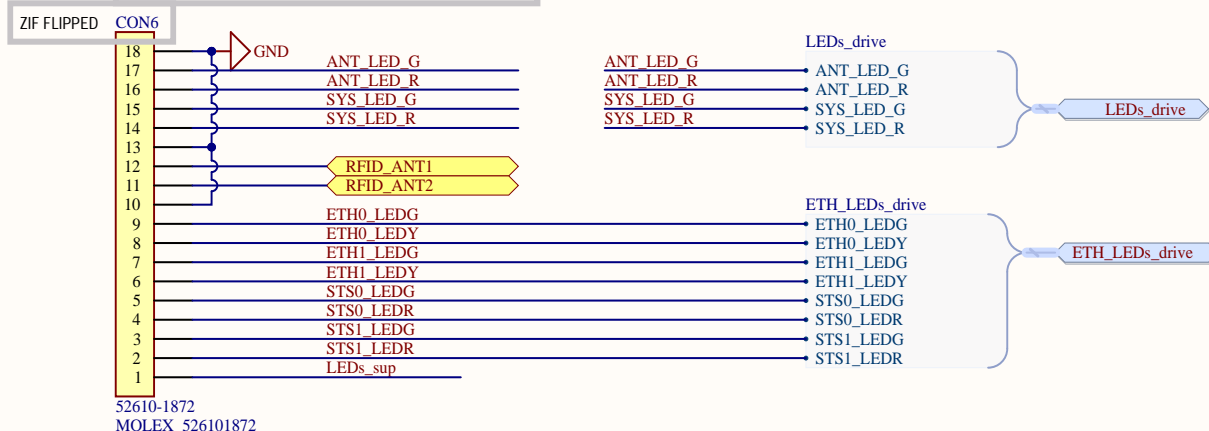


52610-0872
MOLEX 526100871



NO VIAS or TRACES UNDER the IC

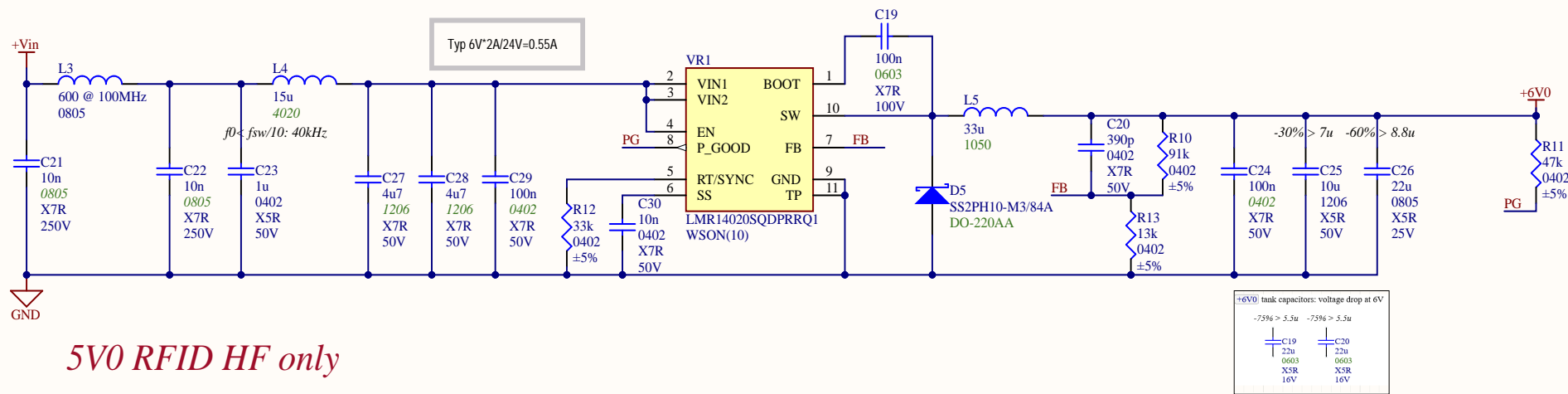
ZIF 18W ANT + ETH / ANT / SYS LEDs to ANT/LED flex PCB



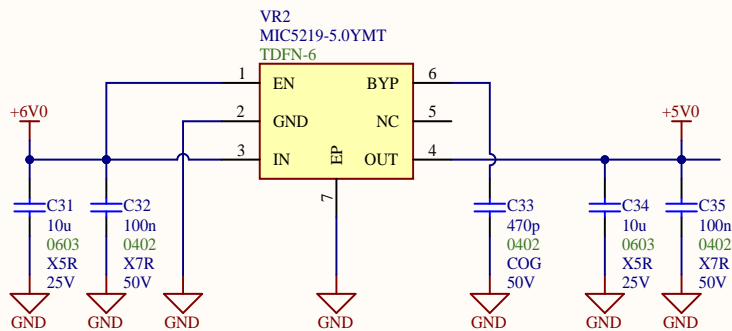
Title: 14B24		Kronotech Srl Via Adriatica, 284 33030 - Basaldella (UD) Italy
Size: A3	Revision: V2	
Date: 11/02/2025	Client: 3 - 6 - 15	

POWER

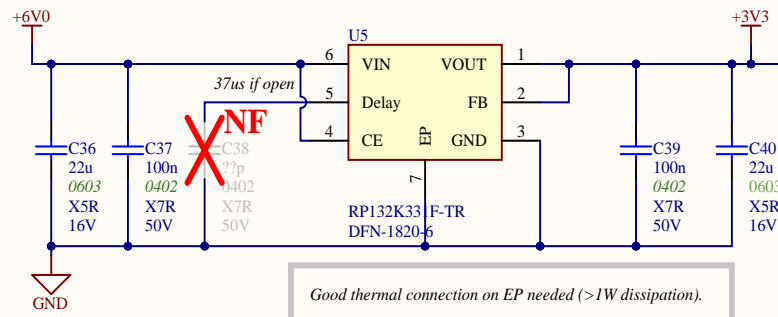
Buck 6V0/2A



5V0 RFID HF only



3V3 / 500mA



POWER BOM:
Notes:
- uC STM: <14mA with active peripherals (SPI, 2xUART, 3xI2C, GPIOs, USB, MEM (FLASH+EEPROM).
- netX90: 350mA w/ SDRAM (13.5mA /30mA erase), FLASH (50mA a tuono)
BOM:
- uC: 15mA
- netX90: 400mA (overall)
- 3xI2C: 6mA
- RTC: <1mA
- IOs : max 6mA (both) + 2*60mA on 5VISO
- EEPROM uC: 3mA
- FLASH uC: 10mA typ (17mA erase)
- RFID: 26mA (350mA AMR) - 3V3 portion only.
- UART-USB: 7mA logic, 15mA typical overall.

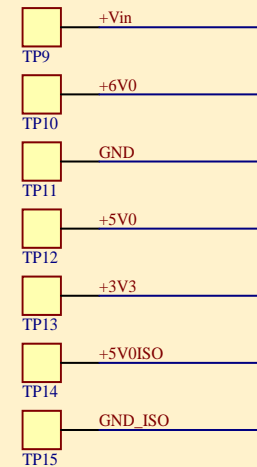
TOTAL: 492mA

Alt. LDOs:
Rth too high:
LT1763 nSOIC8
AP2114HA-3.3TRG1 // LDL1117 SOT223
MIC5219-3.3YM5 sot23-5

OK:
RP132K331F-TR DNF1820-6
ST1L08SPU33R DFN-8
NCP692 DFN-6

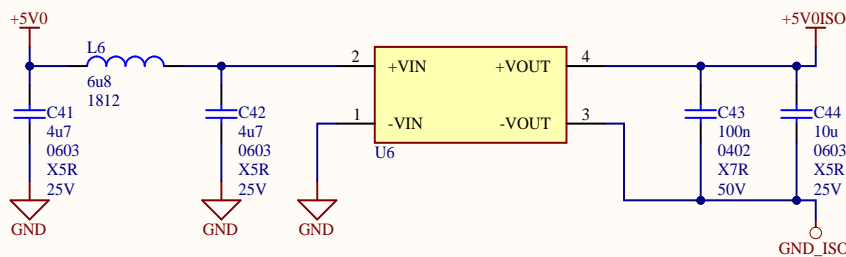
DPAK / DFN (expensive):
LT1764
ISL801031RAJZ-TK (REN)

TEST POINTS POWER

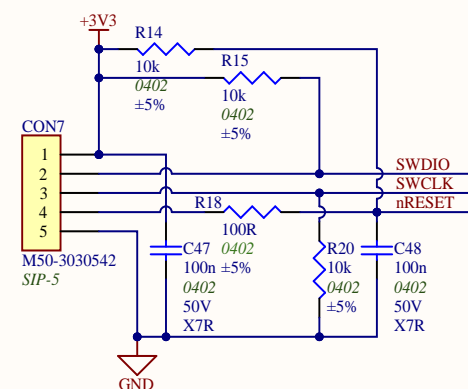
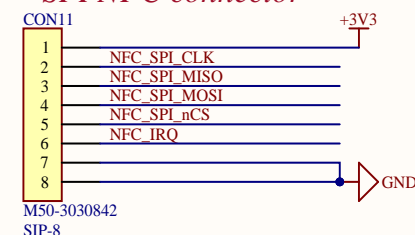


TPs on TOP

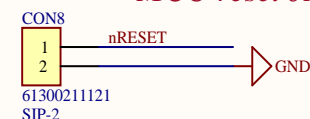
5VISO / 120mA



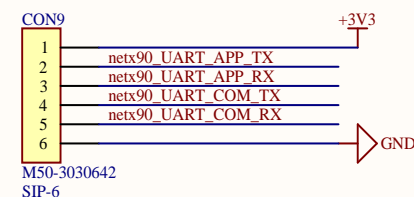
PORTS



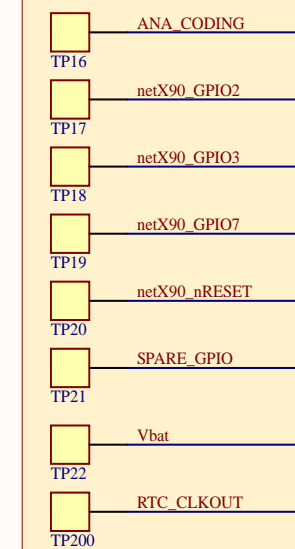
MCU reset JMP



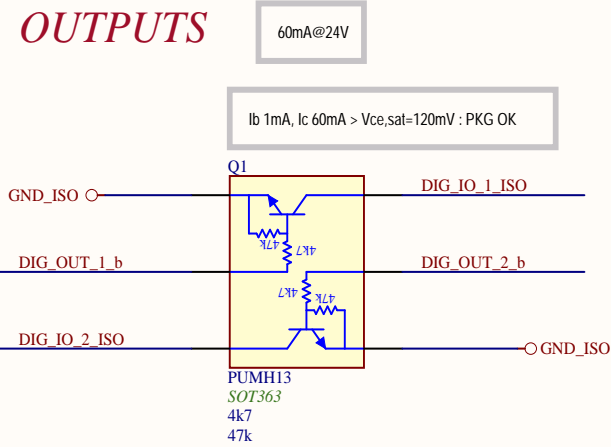
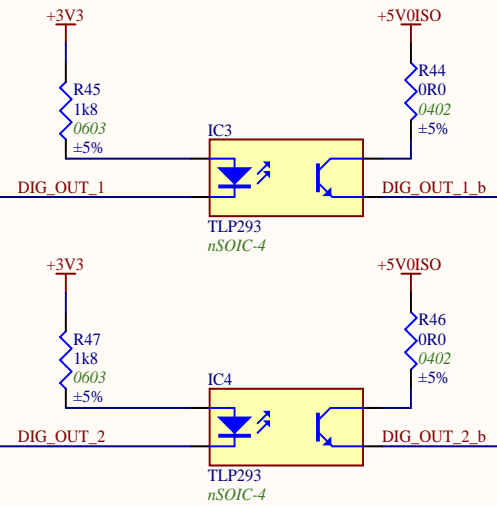
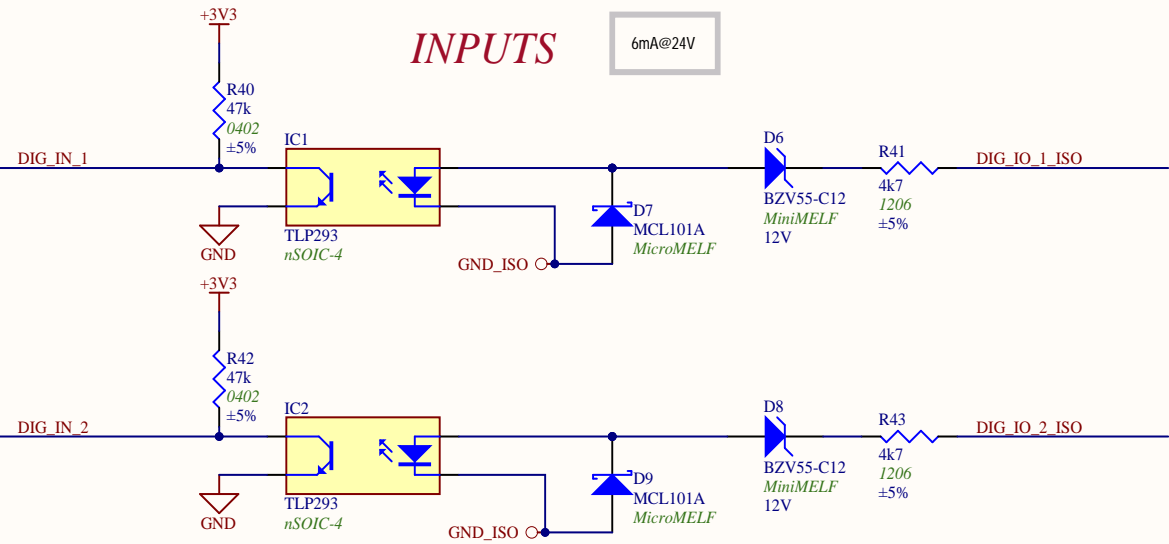
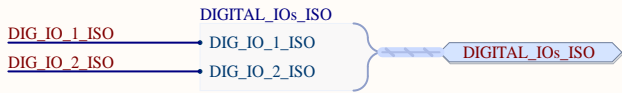
UART COM/APP connector



TEST POINTS MCU



ISOLATED IOs (2+2)

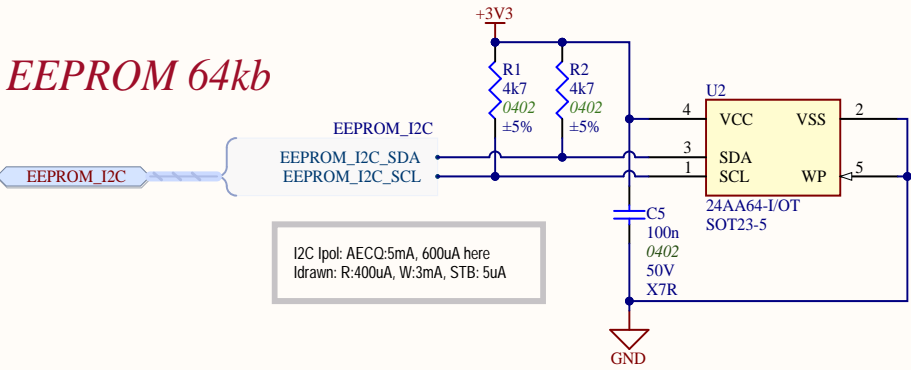


MEMORY

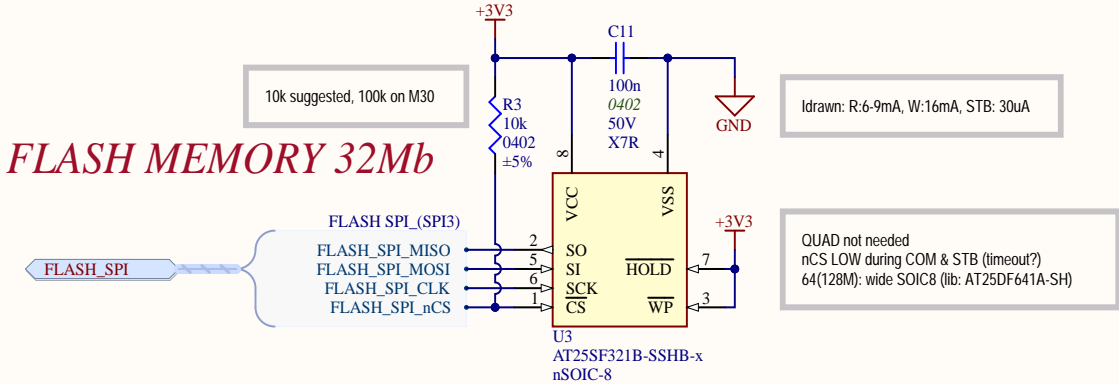
uC

netX90

EEPROM 64kb

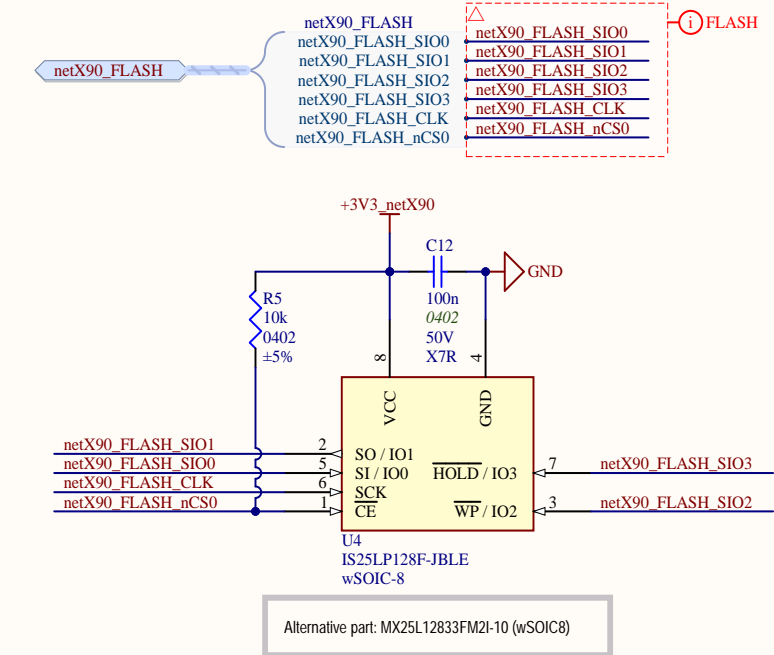


FLASH MEMORY 32Mb



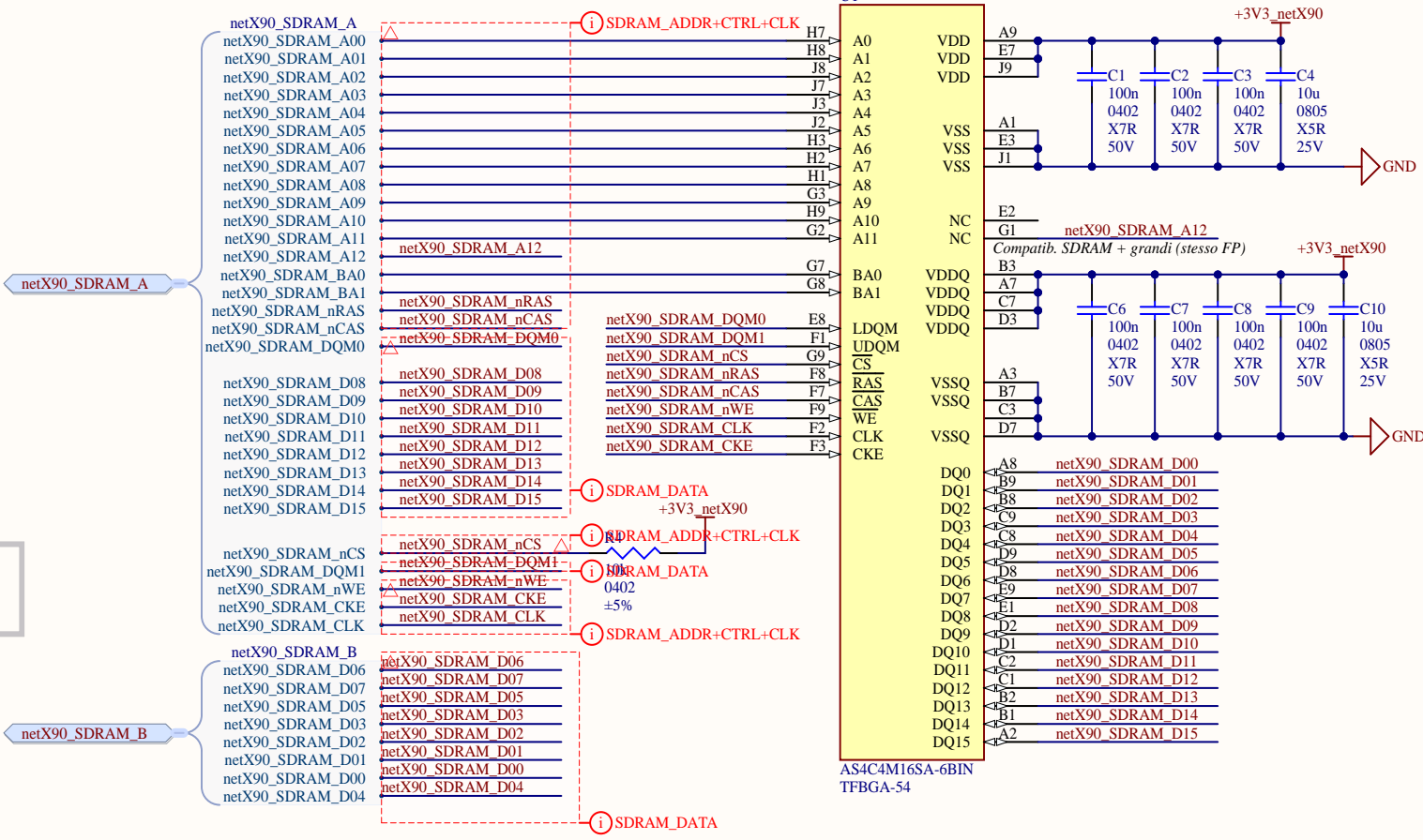
netX90

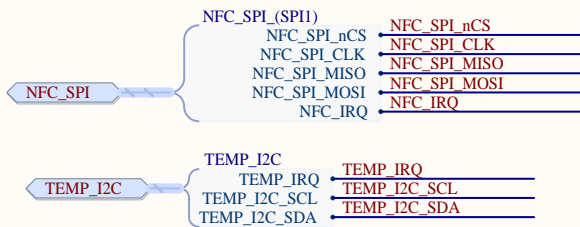
FLASH 128Mbit



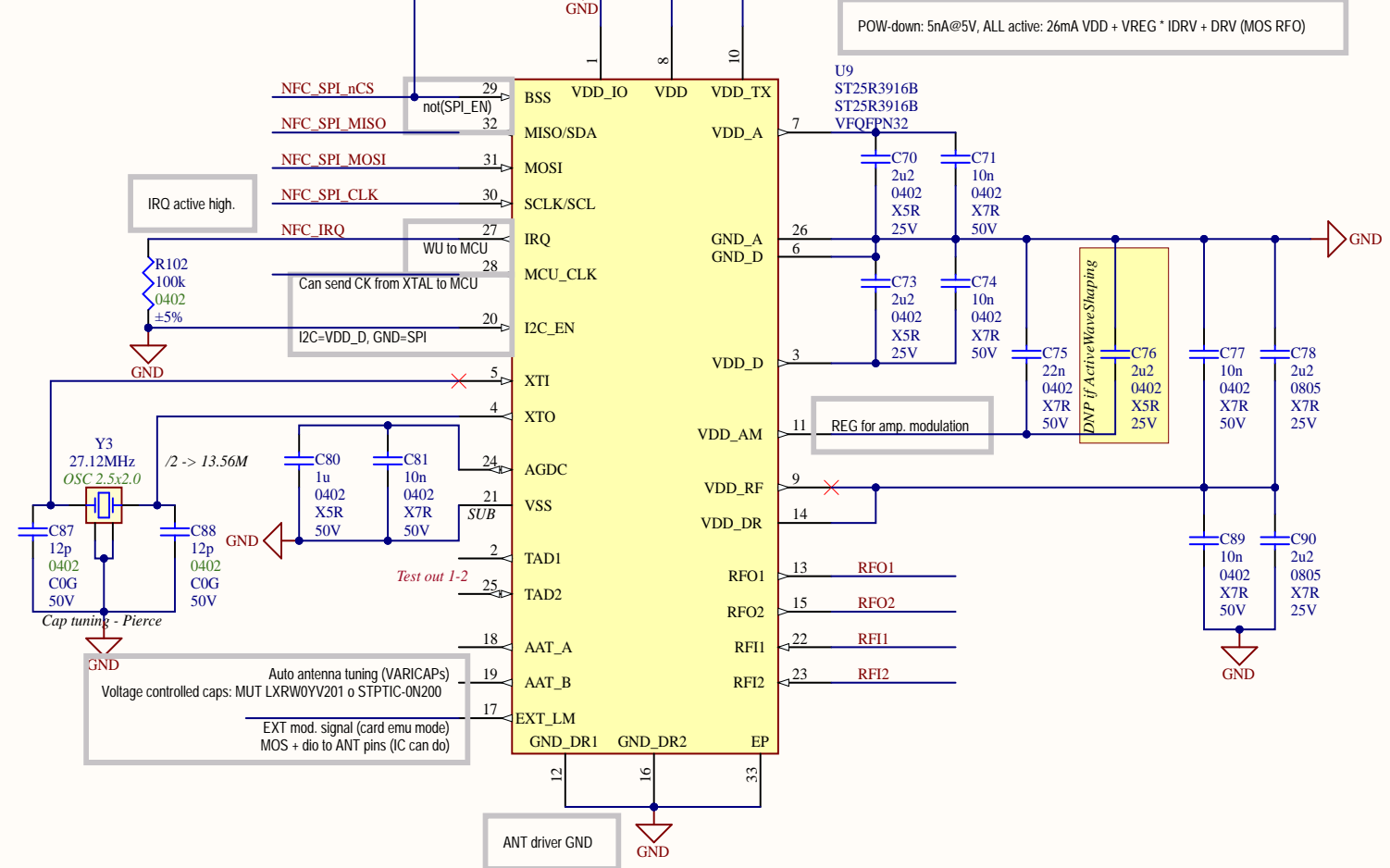
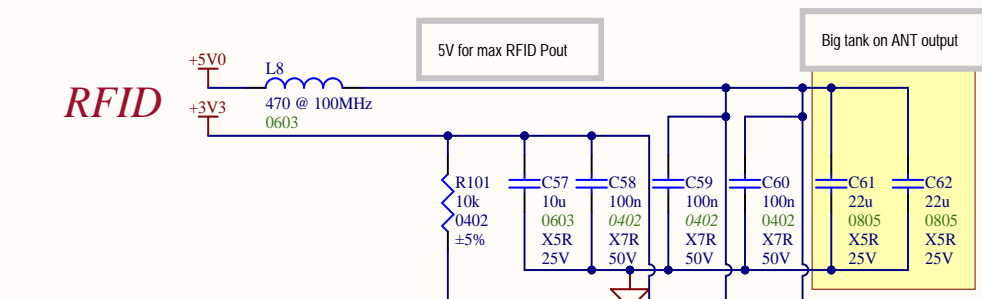
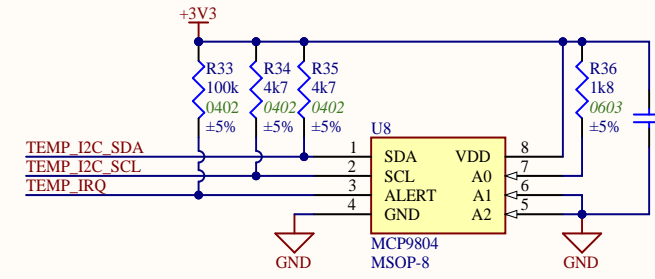
SDRAM 64Mbit

Equalized lines 500hm
Cap nF near Vx e Vss pins (VDD/Q-VSS/Q) - short loop.





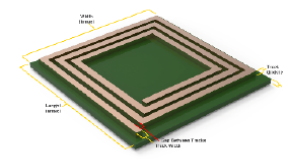
TEMPERATURE SENSING



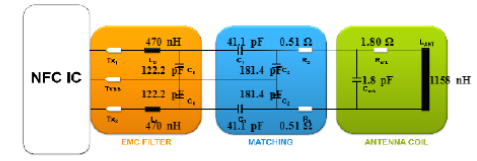
RFID

Length (amax)	81.54	mm
Width (bmax)	74.84	mm
Track width (w)	250	µm
Gap between tracks (g)	300	µm
Additional Overlap Area (A)	0	mm ²
Track Thickness	35	µm
Number of Turns (N)	2	
Turn exponent (E)	1.66	
PCB Thickness	0.125	mm
Er	3.3	

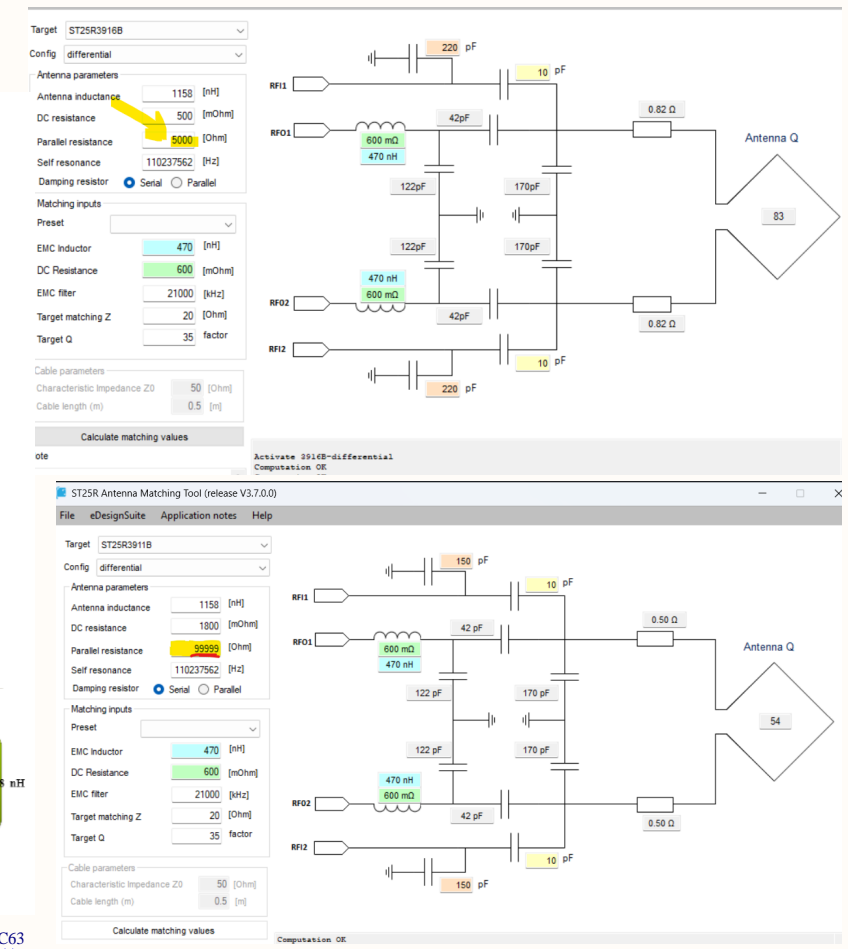
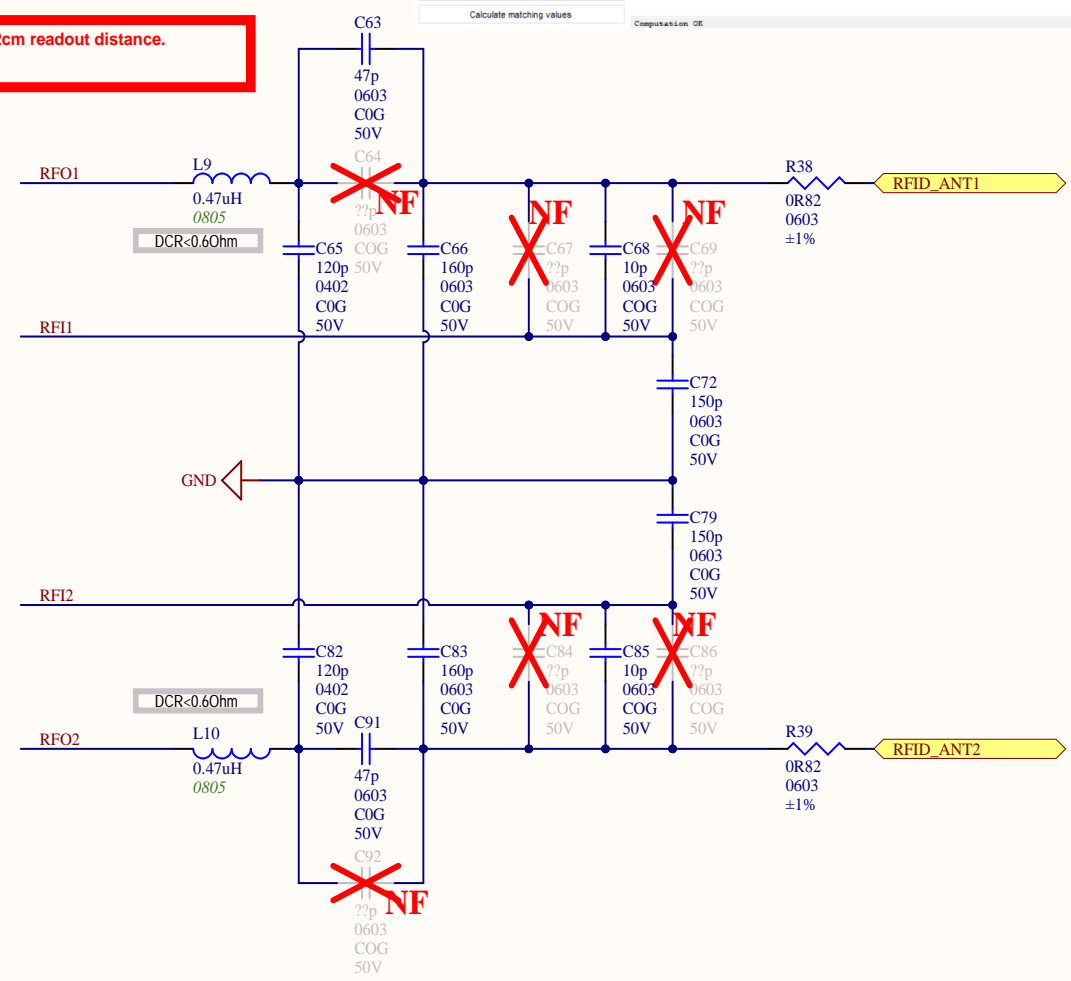
Inductance (Lant)	1158	nH
Lant min	1111	nH
Lant max	1321	nH
Capacitance (Cant)	1.8	pF
Resistance (Rant)	1.80	Ω
Self resonance (Fres)	110	MHz

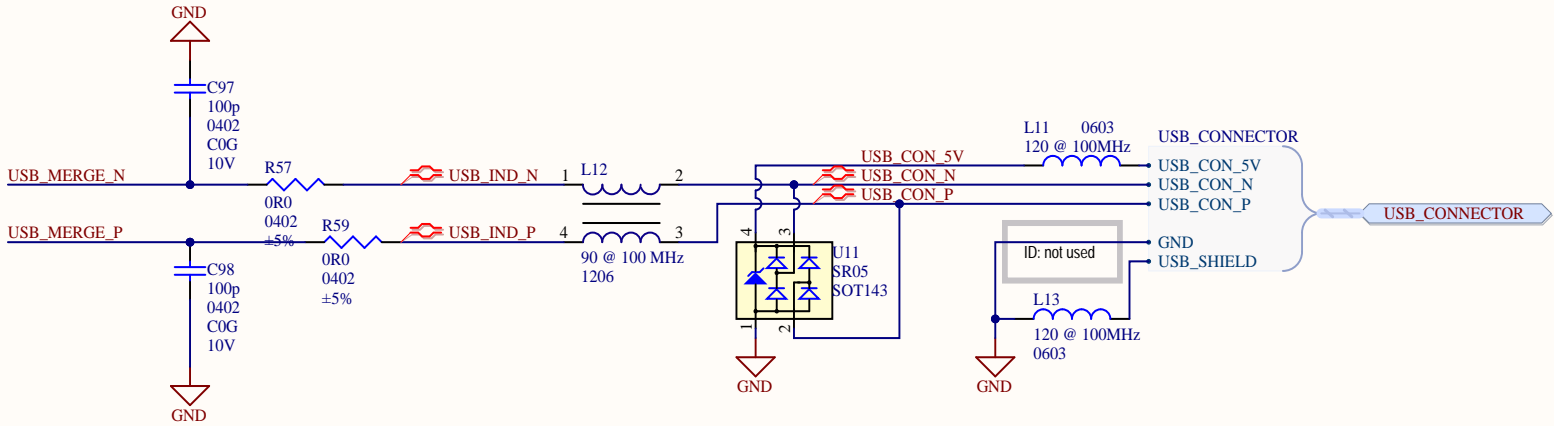


Q	35	
Target impedance	20	Ω
fEMC cut off	21	MHz
L0	470	nH



14A24 with values above: ~12cm readout distance.
To be tuned on 14B24.





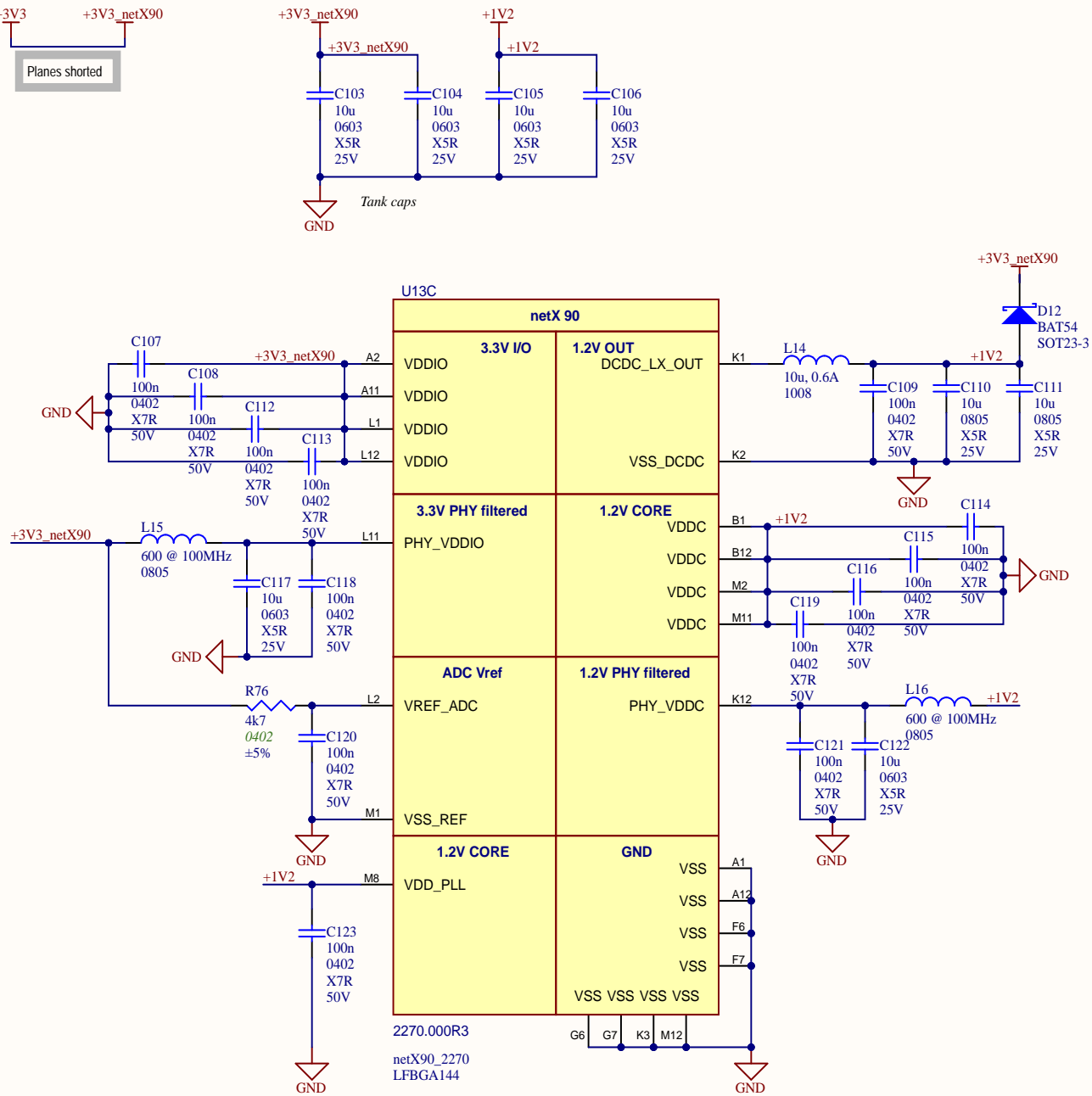
UART to USB FTDI chip removed.

ETHERNET POWER

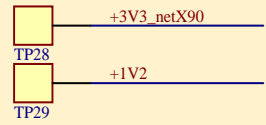
Dissipation 1W: need VIAs to GND.
EP not below whole netX90, just below its center (GND balls) and corners with through vias (out > vias to bot=gnd).

Dimension	Description	mm
c	Clearance	0.1
e	Pitch	0.8
p	Diameter copper pad	0.36
	Diameter solder mask	0.4
	Diameter paste mask	0.32
t	Trace width	0.1
v	Via pad diameter	0.5
w	Via drill diameter	0.1

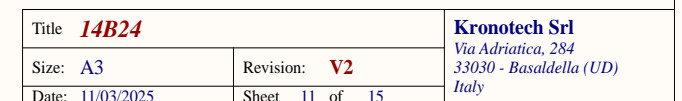
Table 35: VIA dimensions



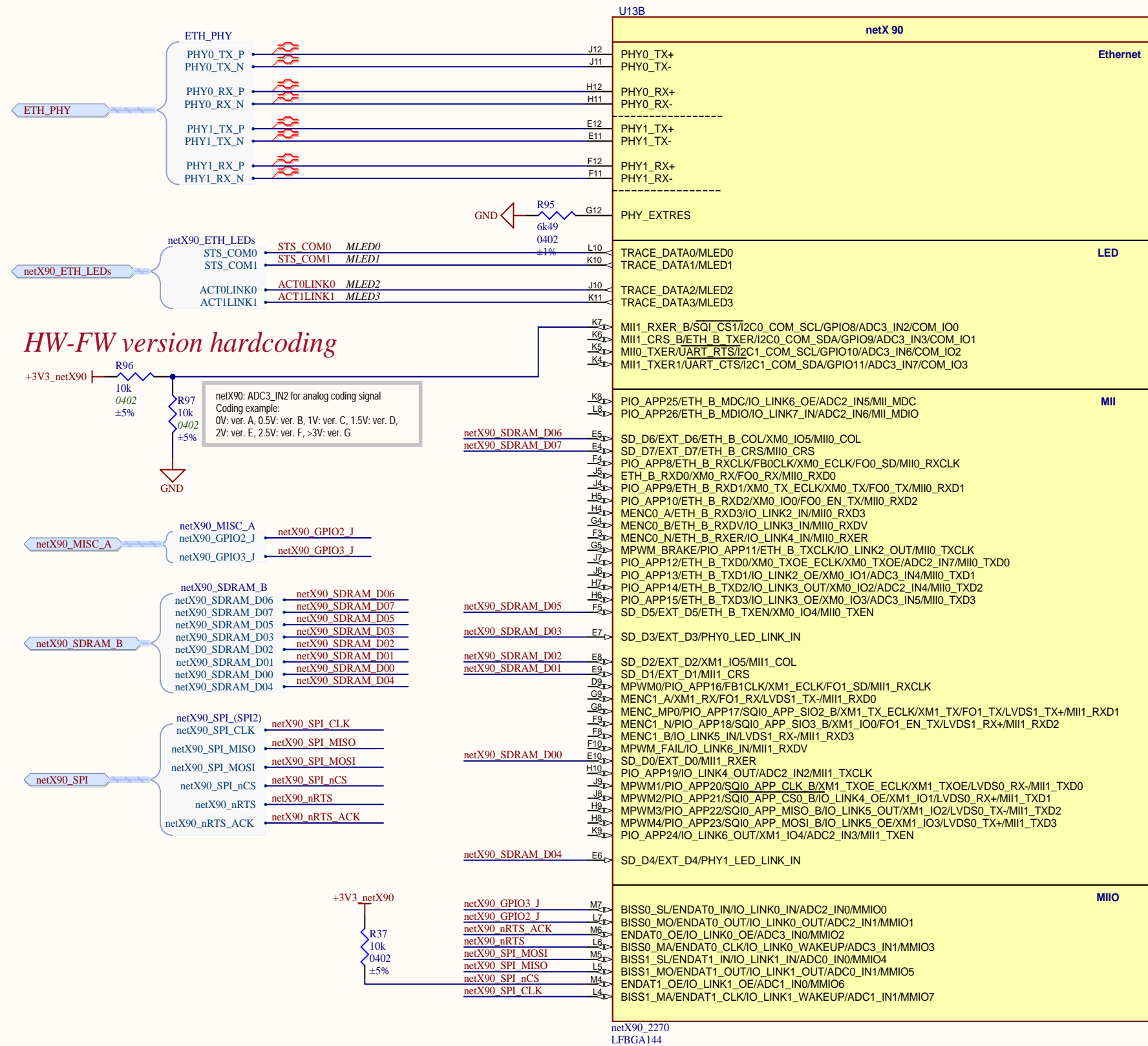
TEST POINTS netX90 POW



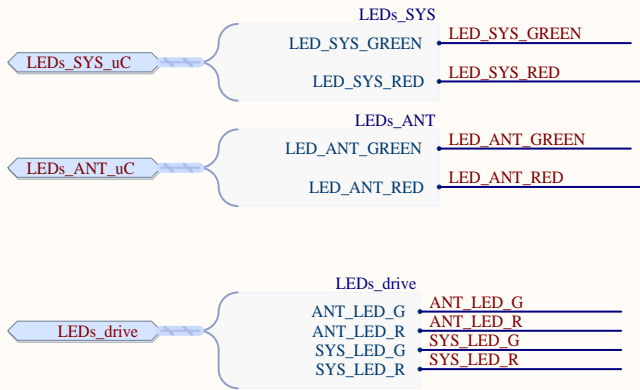
RDY/RUN



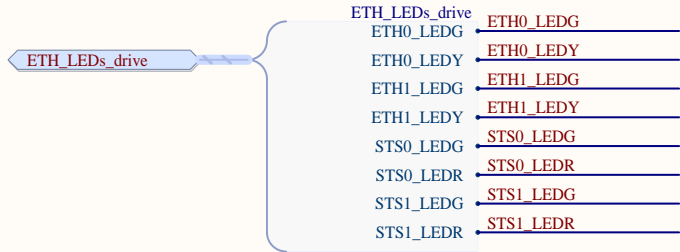
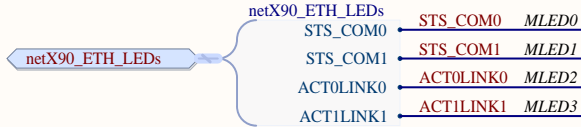
ETHERNET NETX90 2/2



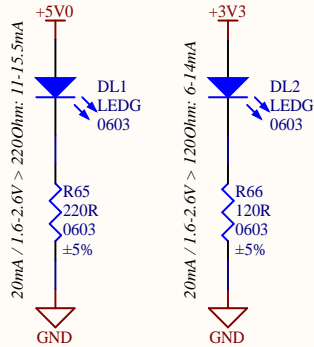
Title 14B24		Kronotech Srl Via Adriatica, 284 33030 - Basaldella (UD) Italy
Size: A3	Revision: V2	
Date: 11/03/2025	Sheet 12 of 15	



LEDs



5V / 3.3V Power

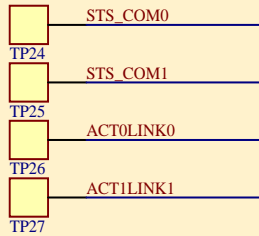


ETH0/1 (+STS) LEDs drive (IND. ETH)

LEDs: 1.8-2.6V@20mA (AMR 15mA@TA=60°C > 100Ohm: 7-15mA target @ 3.3V-VF); GRN LEDs to GND, R/Y to 3V3.



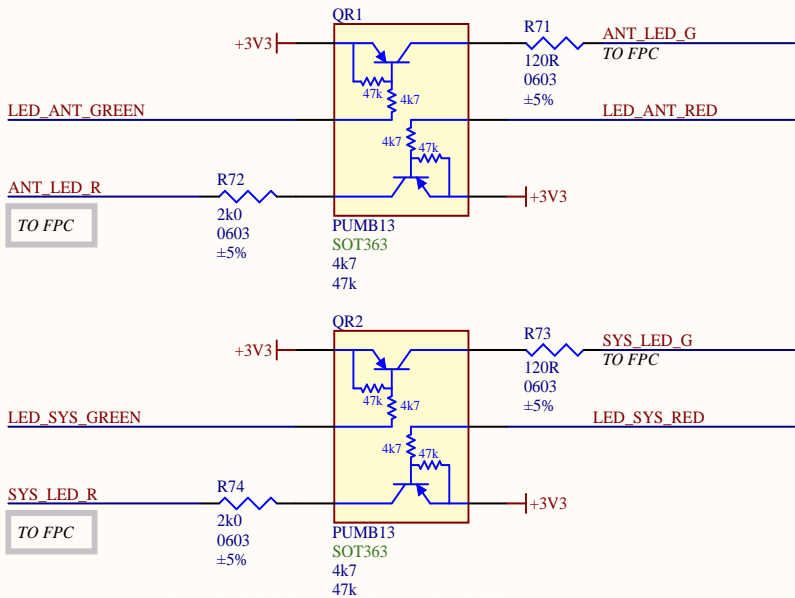
TEST POINTS MLEDs



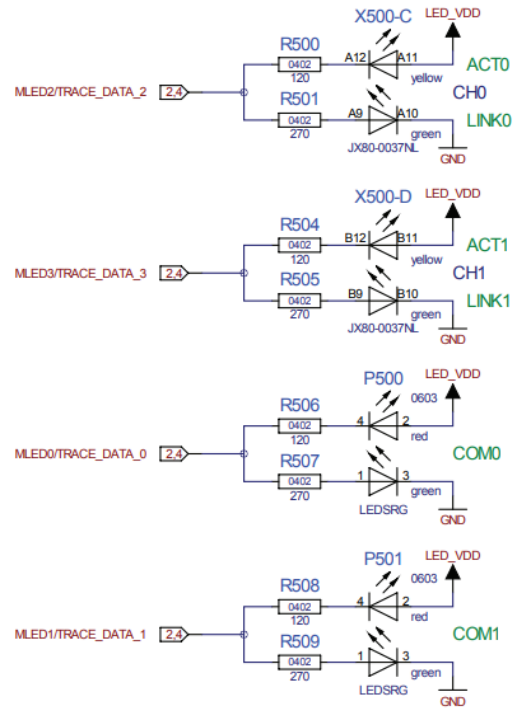
TPs on TOP

SYS / ANT LEDs

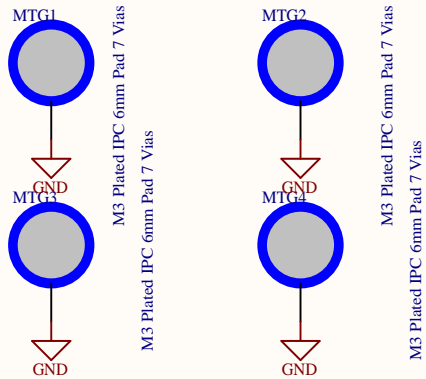
LEDs: 1.8-2.6V@20mA (AMR 15mA@TA=60°C > 100Ohm: 7-15mA target @ 3.3V-VF); all LEDs to GND.



MLEDs



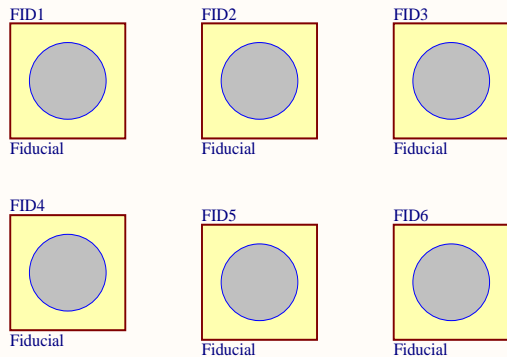
Mounting holes



FIDUCIALS

TOP

BOT



DOC: REVISION HISTORY

14A24 > 14B24:

PCB fixes:

- CON6 (zif TO ANTENNA & LEDs): flipped in the schematic (1>18, 2>17, ...) + tracks swapped on the PCB (layout).
- USBP&USBN were inverted across L12 (CM choke). Fixed and removed anything between uC UART port to FTDI to W2-W3.
- Y2 (ABM11W-48.0000MHZ-7-K1Z-T3) footprint was too big (3.2x2.5) and actually is (2.0x1.6) - 14A24 mounted the small XTAL in the big footprint and it was working. Changed however to 7M-48.000MEEQ-T (3.2x2.5), used on STM eval board to maintain footprint.
- Y5 (netx90 XTAL - XRCGB25M000F1SBBR0) had no PAD4 connection to GND (correction of Crystal-3 symbol & LYT change).
- MTG holes fixed (GND reference added on vias only in LYT - couldn't fix on schematic). Removed poly pours and created MTG* rule to connect directly (no thermal reliefs).
- SYS, ANT LED resistors: aligned to 03B24 values to match R/G luminosity: R72,R74: 100>2kOhm, R71,R73: 100>120Ohm.

Other improvements:

>>> ETH (17x24): CON3, CON5 common bounding network changed from GND to PE. PE region (PE signal on ZIF CON3,CON5, replacing GND) at the bottom right of the board has been extended up to ETH XFRs on power layers (2,3,5), Such layers are empty below the ETH XFRs. JST ZIFs removed (CON4, CON17), as 17B24 is now bringing PE from M12 external braid. W200, R200, C200 added to provide RC filtering PE-GND.

Block diagram updated.

- Dip switches (S1 and S2) replaced by 10k Rpu/Rpd for digital coding (static). BOM will define versions. Added R103,4,5 (uC), R106,7,8 (netX90) between pin and GND.
- UART-USB (FTDI PART) from MCU removed, down to W2 & W3 + USB ZIF. Removed CON2, U12 (FTDI), R60, C99, C100, C101, C102, W2, W3. Removed nets: USB_N, USB_P, USB_UART_RX, _TX, _nCTS, _nRTS. Using internal USB on STM32G0B0RE.
- I2C-ext. RTC part from MCU to PCF2131TF (R-D-C+batt to Vbat_uC) removed. Removed R48, R49, R50, R51, R52, C93, C94, C95, U10 (PCF2131TF), CON13 (RTC CLKOUT), CON12 (JMP RTC int/ext). Removed nets: RTC_SCL, RTC_SDA, RTC_IRQ, Vbat_RTC. Removed ideal diode circuit (Q2, Q3, W1, TP23, R54, R55). [06] RTC BATTERY sheet removed (RCD and battery holder embedded into [05] MCU sheet). Using internal RTC on STM32G0B0RE.
- CON100 & TP200 & R201: RTC CLKOUT (PA4, pin21) added for RTC tuning - NFC_SPI_nCS moved from PA4 to PA3 (pin20). R201: 10k pull down RTC CLKout to GND. ICD and block diagram updated.
- 3V3 merged with 3V3_netx90 supply lines > R75 removed and +3V3 = +3V3_netX90. Recreated a single poly region on L3 (+3V3 layer).
- Layout updates: TOP GND and vias stitching on emptied areas, GND_ISO on the bottom left of the PCB was replicated and stitched with vias on L2 and L4, fixed a bunch of silk issues, small displacement of passives and PE/GND stitching around ETH lines, accordions added between netX90 and related FLASH memory.
- Layer stackup updated based on supplier's PDF and S50, D90, D100 calculated. Impedance error about 12% in the worst case. FAB notes on layout (stackup, FR4 material, finish and colors).
- 'netX90 SDRAM rules fixed, netX90 SDRAM and FLASH tracks modified to match constraints.

Notes:

- Y4 does not exist (XTAL out of page which was then removed after annotating).
- MTG1-4 vias are not connected to GND on schematics + Supply nets cannot be set on schematics --> need to maintain these differences against layout.

V0 > V1:

HF antenna: tuning circuit added and related componets marked as fitted.

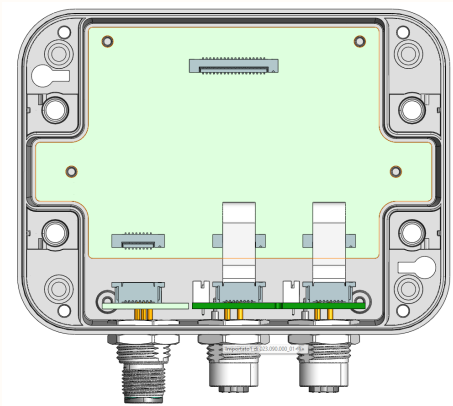
Updated provisionally red LED resistor values for red ETH LEDs (0402). RED curemnt level decreased (120>4700hm) to balance lumi and get rid of slight glow when ANT is ON.

V1 > V2:

- STS0/1 red LEDs tuning: R62, R68: 4700hm > 2kOhm. Layout: fixed M5 designators (assembly) to fit tihe component outline (0.4mm & inside the box).

LYT:
6 layers
through vias, 0.2mm min (below netX90).
Keepout bottom 6mm (no cpts on bottom foreseen).

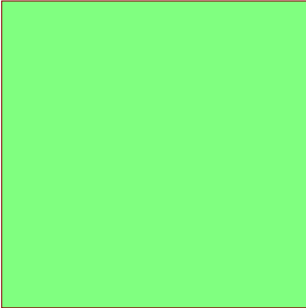
BUS by speed:
UARTs: 250kHz
I2C: 400kHz
SPIs: 6.25MHz (+ related GPIOs)
USB: 12MHz
ETH: 10/100M
SDRAM: 166MHz



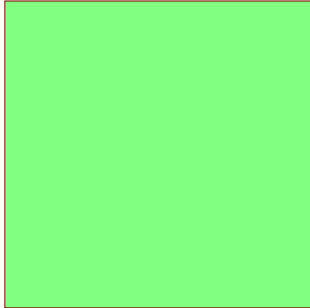
BOTTOM KEEPOUT:

6mm max height for cpts

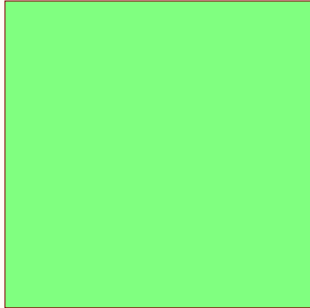
Designator
[01] - COVER PAGE.SchDoc



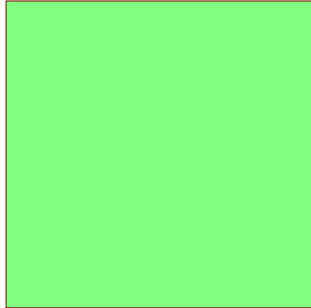
Designator
[02] - BLOCK DIAGRAM.SchDoc



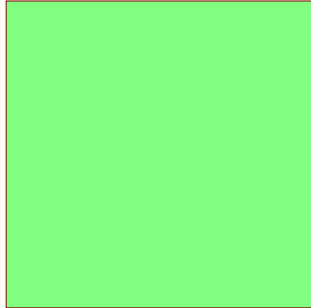
Designator
[03] - CONNECTORS.SchDoc



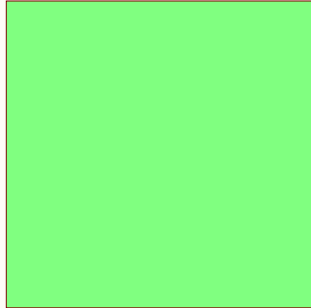
Designator
[04] - POWER.SchDoc



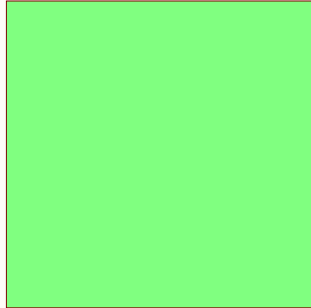
Designator
[05] - MCU.SchDoc



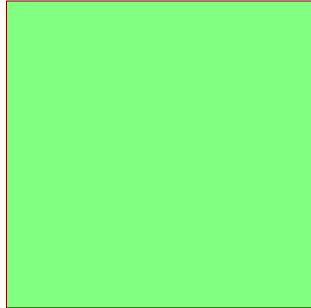
Designator
[06] - IOs.SchDoc



Designator
[07] - MEMORY.SchDoc



Designator
[08] - RFID TEMP sensor.SchDoc



TEMPLATE NOTES

Set Project Parameters

- 1) Go to Project -> Project Options -> Parameters
- 2) Set Project and Version

Mark Not Fitted Components as

NF

Net Class Example



Differential signal example



TITLE Examples (You can change the color to reflect your company color)

PAGE TITLE

Peripheral / Group of component title

Smaller Ttitle

Schematic Status Explanation

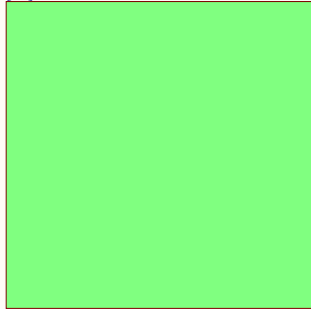
DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

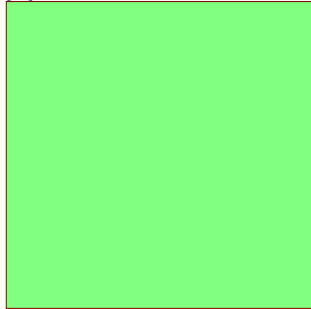
CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

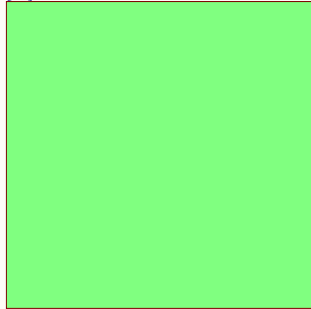
Designator
[09] - USB.SchDoc



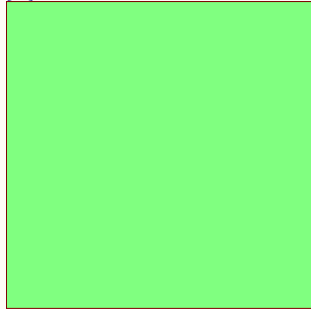
Designator
[10] - ETHERNET NETX90 POW.SchDoc



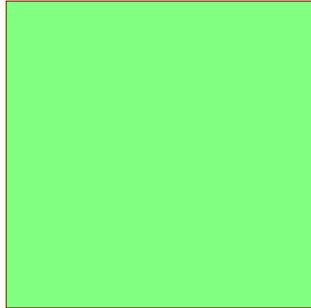
Designator
[11] - ETHERNET NETX90 2.SchDoc



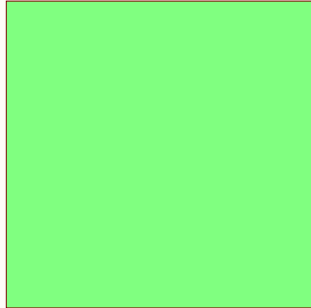
Designator
[12] - ETHERNET NETX90 3.SchDoc



Designator
[13] - LEDs.SchDoc



Designator
[14] - DOC REVISION HISTORY.SchDoc



Title I4B24		Kronotech Srl <i>Via Adriatica, 284</i> <i>33030 - Basaldella (UD)</i> <i>Italy</i>
Size: A3	Revision: V2	
Date: 11/03/2025	Sheet 15 of 15	