
Ethernet Compliance Testing for 10BASE-T, 100BASE-TX, and 1000BASE-T

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INTRODUCTION

The IEEE 802.3 Ethernet Compliance testing encompasses a wide range of tests that utilize different waveforms for the various device speeds:

- 10BASE-T: Four waveforms (link pulse/idle, pseudo-random, all ones, and arbitrary waveform signal)
- 100BASE-TX: Two waveforms (transmit scrambled idle and arbitrary waveform signal)
- 1000BASE-T: Five waveforms (four test mode 1-4 waveforms and arbitrary waveform signal)

The register settings apply to the PHY registers for most of Microchip's Ethernet products.

Note: The test setup and figures are with a Tektronix scope, TDSET3 Ethernet Compliance Software, and TF-GBE test fixture board. The Twisted Pair Model (TPM) is on the test fixture board.

10BASE-T COMPLIANCE TESTING

The 10BASE-T compliance tests are:

- Link Pulse Testing
- Medium Attachment Unit (MAU)
- TP_IDL
- Jitter
- Differential Voltage
- Harmonics
- Transmitter Return Loss
- Receiver Return Loss
- Common-Mode Voltage

Link Pulse Testing and TP_IDL are tested with and without the Twisted Pair Model. Each test section below provides the test description, test setup details, and pass criteria.

For 10BASE-T test data transmission (pseudo-random and all ones patterns) on KSZ switches, KSZ Gigabit PHYs and LAN PHYs (other than LAN78xx which can generate test patterns itself), use the link partner (set to forced 10BASE-T) to transmit the signal to the device under test (DUT) and enable remote loopback on the DUT.

For 10BASE-T test data transmission (pseudo-random and all ones patterns) on KSZ80xx PHYs, the PHY is connected to the MAC of a switch via MII/RMII connection. The link partner transmits the test signal to the switch's PHY port and through the MII/RMII to the DUT's PHY port.

Link Pulse Testing

This is a test of the 10BASE-T Link Pulse signal integrity.

For link pulse testing without Twisted Pair Model, the DUT is connected to the DUT port for the 10BASE-T Parametric/Template Test (some boards may add 'without Twisted Pair Model'), and the oscilloscope probe is attached to the test jumper.

For link pulse testing with Twisted Pair Model, the DUT is connected to the DUT port for the 10BASE-T Parametric/Template Test with Twisted Pair Model, and the oscilloscope probe is attached to the test jumper after load selection.

To configure the DUT for link pulse testing, refer to [10BASE-T Link Pulse Setting on any part](#) for register settings. Pass specification is based on the Link Pulse remaining inside the mask for both the head and the tail.

FIGURE 1: 10BASE-T LINK PULSE WITHOUT TWISTED PAIR MODEL

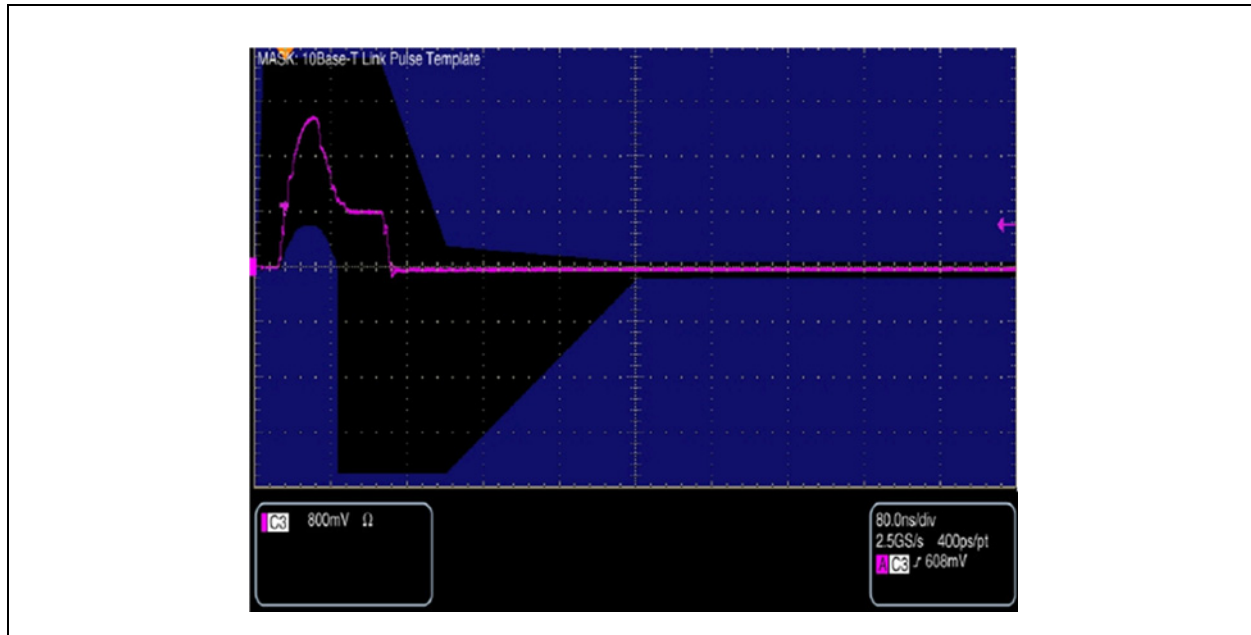
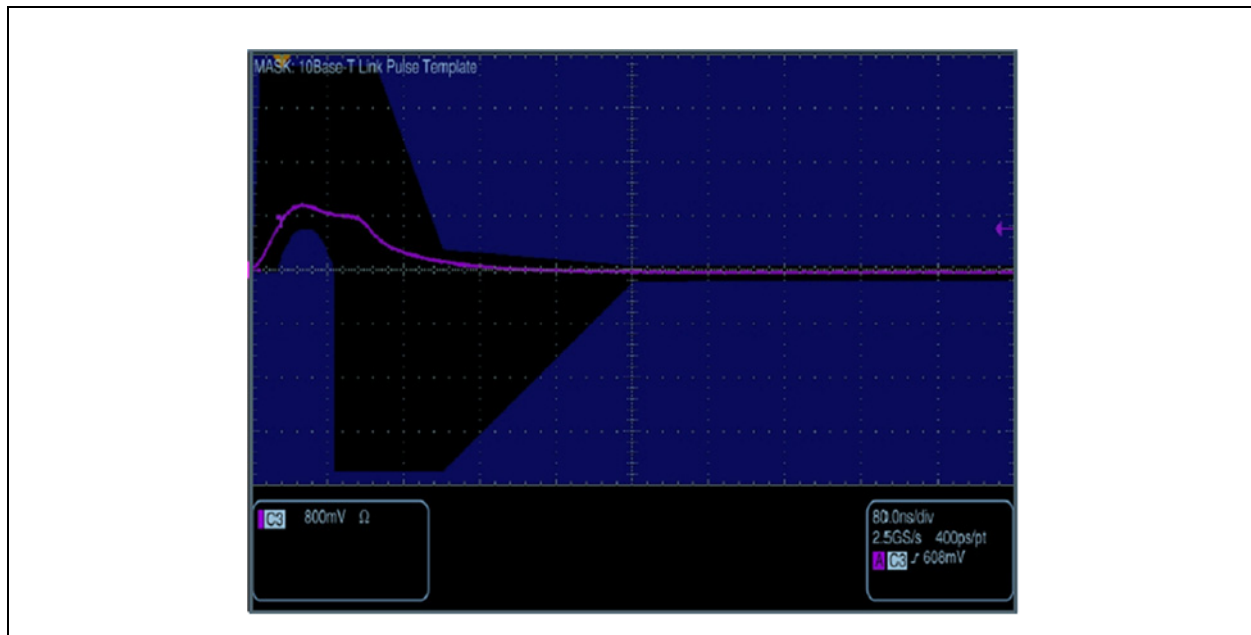


FIGURE 2: 10BASE-T LINK PULSE WITH TWISTED PAIR MODEL



Medium Attachment Unit (MAU)

This is a test of the MAU of the PHY. The DUT is connected to the DUT port for the 10BASE-T Parametric/Template Test with Twisted Pair Model, and the oscilloscope probe is attached to the test jumper. To configure the DUT for MAU testing, refer to the [10BASE-T Loopback Mode on KSZ parts](#) register settings. For LAN78xx, refer to [10BASE-T Pseudo-Random Signal Setting – LAN78xx](#) for register settings. On the oscilloscope, set for internal or external. Short the 100-ohm jumper on the test board. Pass specification is based on the signal remaining inside the mask.

FIGURE 3: 10BASE-T MAU - EXTERNAL

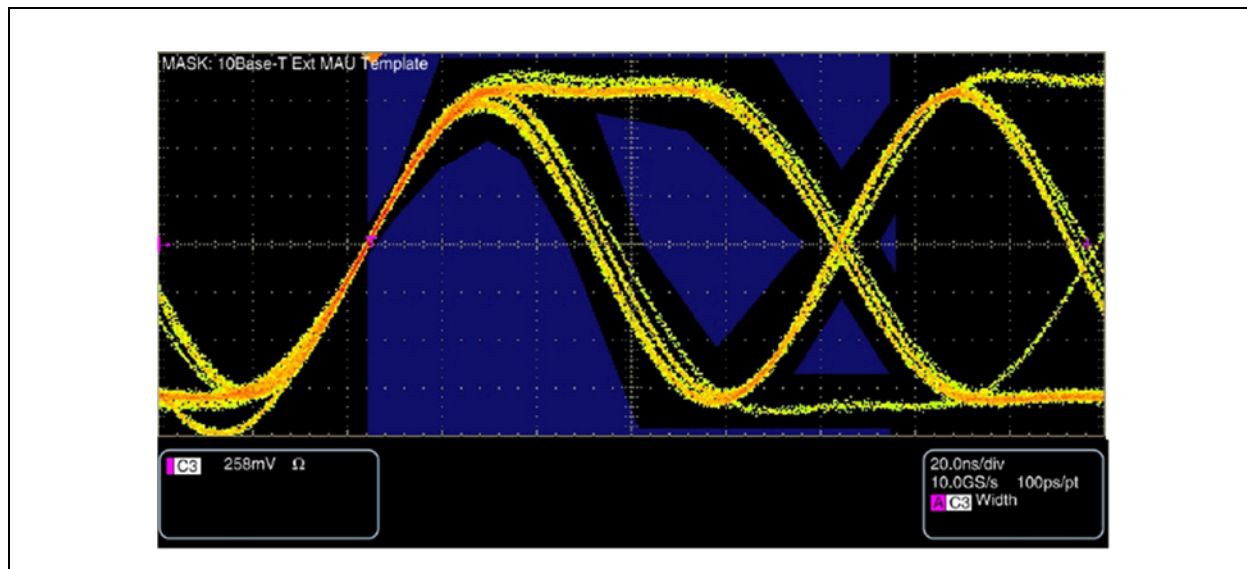
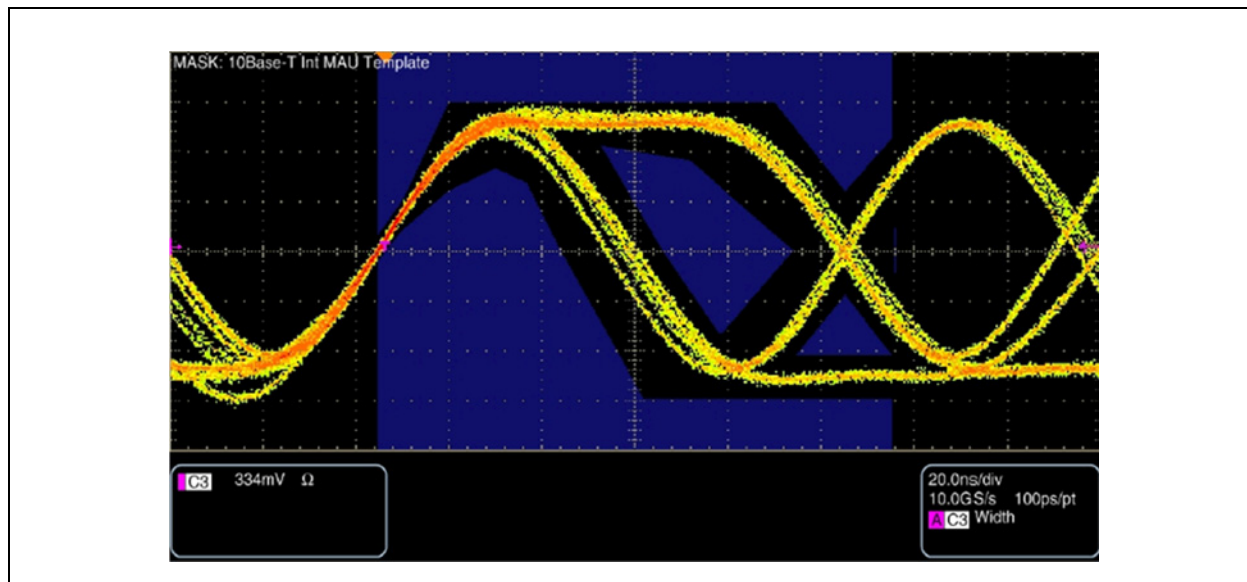


FIGURE 4: 10BASE-T MAU - INTERNAL



TP_IDL

This is a test of the 10BASE-T TP_IDL signal at the end of a data packet, which signals the start of the idle period.

For TP_IDL without Twisted Pair Module, the DUT is connected to the DUT port for the 10BASE-T Parametric/Template Test (some boards may add 'without Twisted Pair Model'), and the oscilloscope probe is attached to the test jumper.

For TP_IDL with Twisted Pair Module, the DUT is connected to the DUT port for the 10BASE-T Parametric/Template Test with Twisted Pair Module, and the oscilloscope probe is attached to the test jumper.

To configure the DUT for TP_IDL testing, refer to the [10BASE-T Loopback Mode on KSZ parts](#) register settings. For LAN78xx, refer to [10BASE-T Pseudo-Random Signal Setting – LAN78xx](#) for register settings. Pass specification is based on the TD_IPL remaining inside the mask.

FIGURE 5: 10BASE-T TP_IDL WITHOUT TWISTED PAIR MODEL

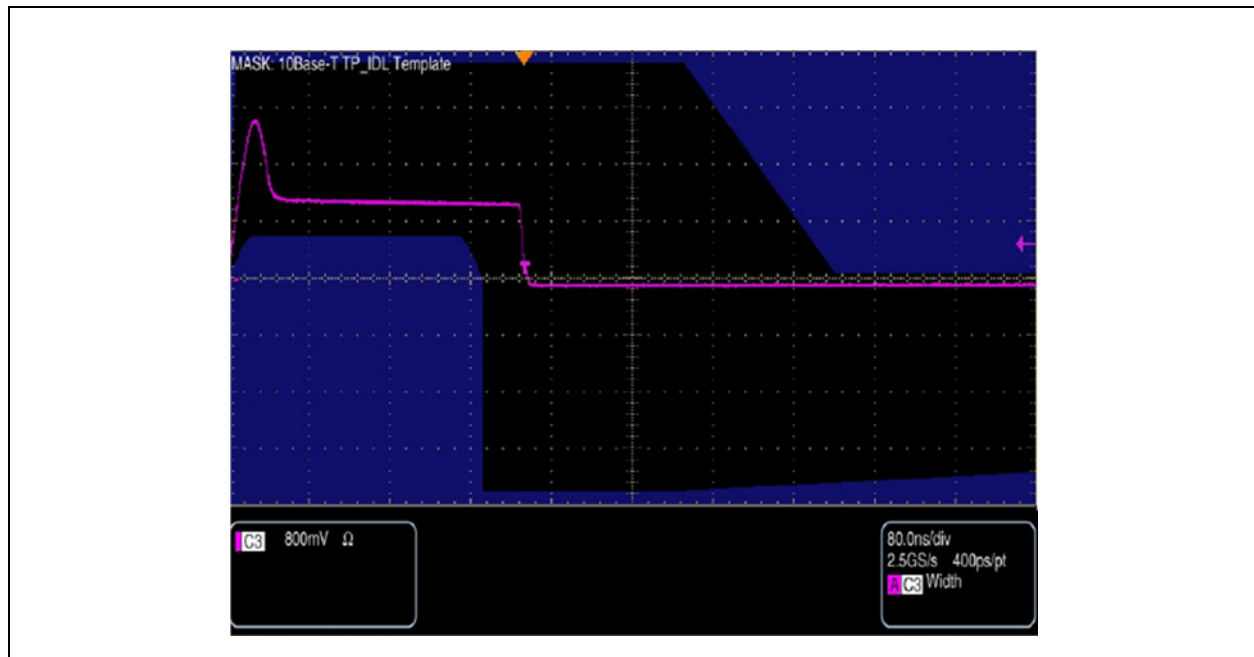
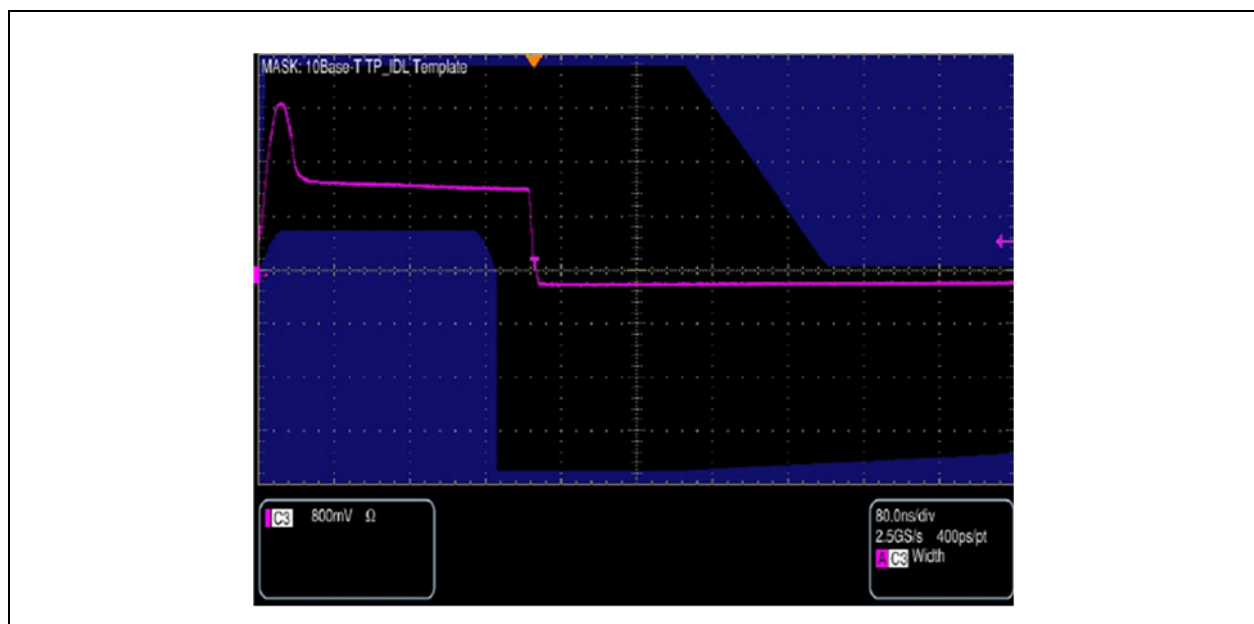


FIGURE 6: 10BASE-T TP_IDL WITH TWISTED PAIR MODEL



Jitter

This is a test of the 10BASE-T link data pattern for jitter.

For jitter without Twisted Pair Module:

- The DUT is connected the DUT port for the 10BASE-T Parametric/Template Test (some boards may add 'without Twisted Pair Model'), and the oscilloscope probe is attached to the test jumper.
- Pass specification is based on the jitter at both 8 bit times and 8.5 bit times crossovers less than ± 20 ns.

For jitter with Twisted Pair Module:

- The DUT is connected to the DUT port for the 10BASE-T Parametric/Template Test with Twisted Pair Model, and the oscilloscope probe is attached to the test jumper.
- Pass specification is based on the jitter at both 8 bit times and 8.5 bit times crossovers less than ± 11 ns.

The Link Partner is connected to the other Ethernet port. To configure the DUT for jitter testing, refer to the [10BASE-T Loopback Mode on KSZ parts](#) register settings. For LAN78xx, refer to [10BASE-T Pseudo-Random Signal Setting – LAN78xx](#) for register settings.

FIGURE 7: 10BASE-T 8.5 BIT TIME JITTER WITHOUT TWISTED PAIR MODEL

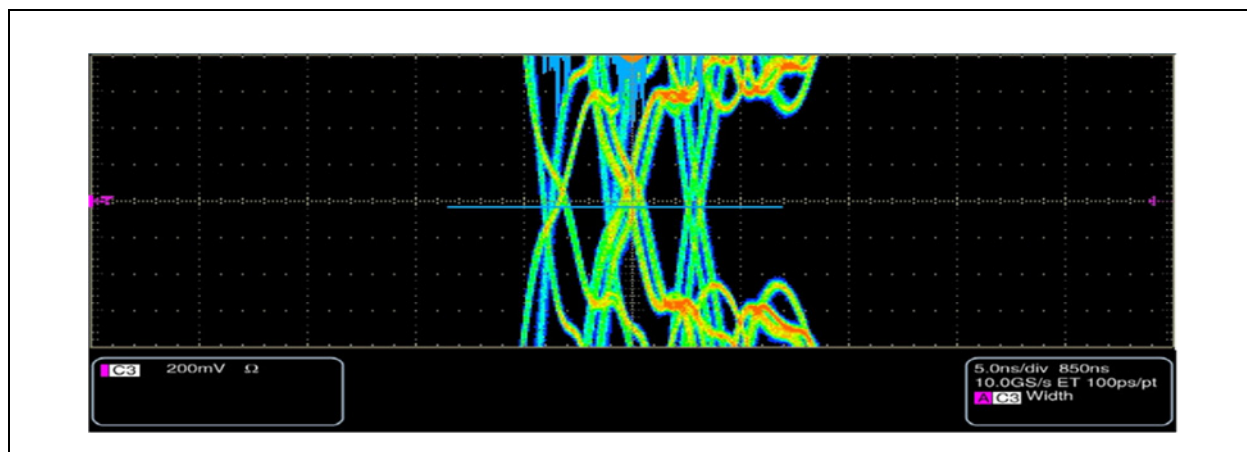
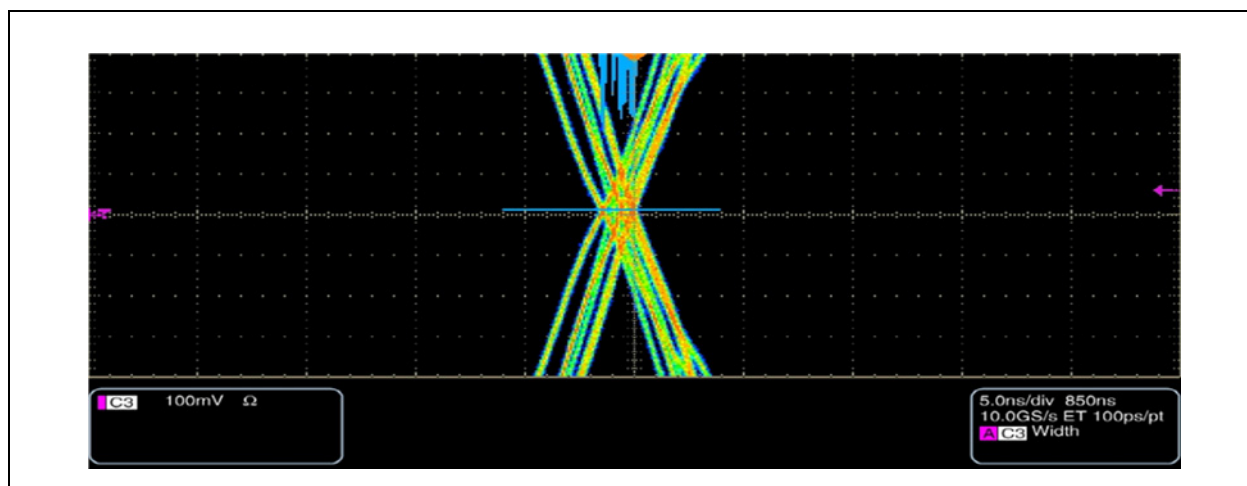


FIGURE 8: 10BASE-T 8.5 BIT TIME JITTER WITH TWISTED PAIR MODEL



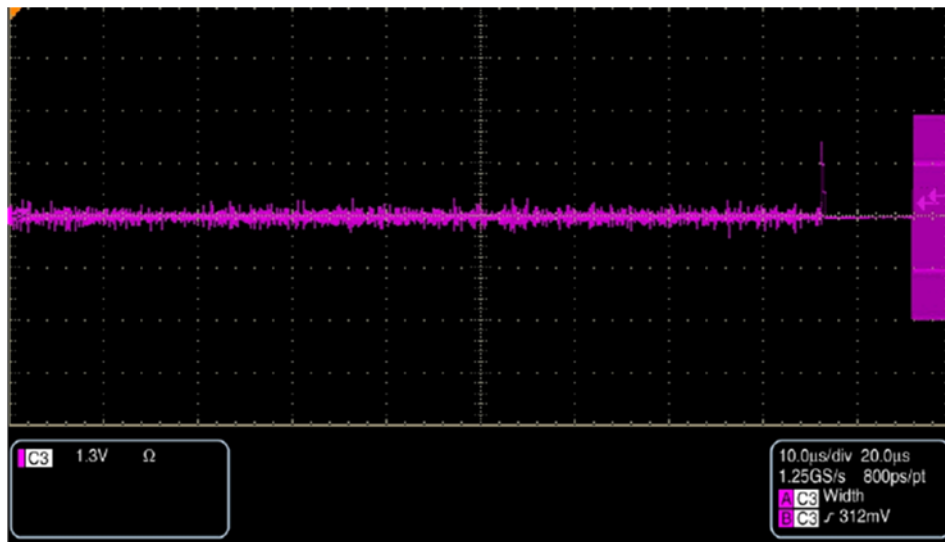
Differential Voltage

This is a test of the peak differential voltage of the 10BASE-T signal. The DUT is connected to the DUT port for the 10BASE-T Parametric/Template Test, and the oscilloscope probe is attached to the test jumper. The Link Partner is connected to the other Ethernet port. To configure the DUT for differential voltage testing, refer to the [10BASE-T Loopback Mode on KSZ parts](#) register settings. For LAN78xx, refer to [10BASE-T Pseudo-Random Signal Setting – LAN78xx](#) for register settings.

Pass specification is based on the following:

- V_{min} : -2.8V to -2.2V
- V_{max} : +2.2V to +2.8V

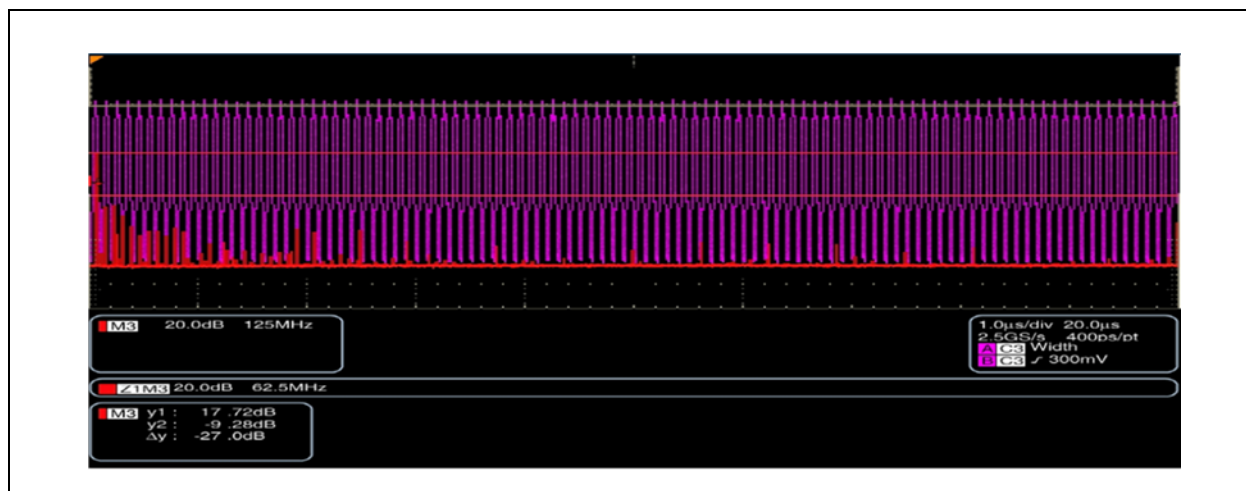
FIGURE 9: 10BASE-T DIFFERENTIAL OUTPUT VOLTAGE



Harmonic Distortion

This is a test of the harmonic distortion of the 10BASE-T signal. The DUT is connected to the DUT port for the 10BASE-T Parametric/Template Test, and the oscilloscope probe is attached to the test jumper. The Link Partner is connected to the other Ethernet port. To configure the DUT for harmonic distortion testing, refer to the [10BASE-T Loopback Mode on KSZ parts](#) register settings. For LAN78xx, refer to the [10BASE-T All Ones Signal for Harmonic Distortion – LAN78xx](#) for register settings. Pass specification is based on all harmonics being more than 27 dB less than the fundamental signal.

FIGURE 10: 10BASE-T HARMONIC DISTORTION

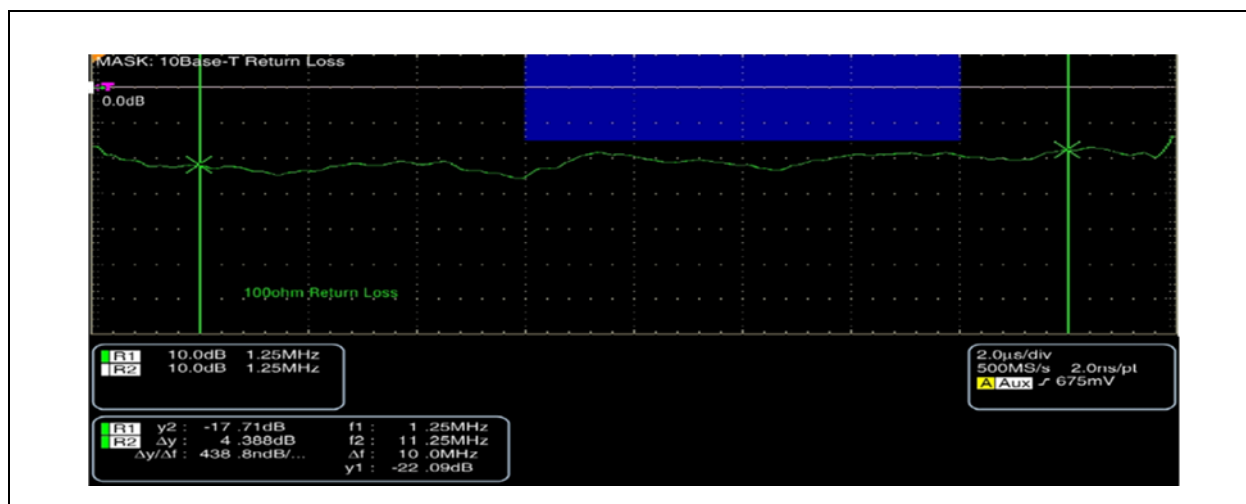


Transmitter Return Loss

This is a test of the transmitter return loss. A differential signal (positive and negative) must be provided externally from a waveform generator to the test board. The differential signal is fed back to the oscilloscope running the return loss measurements. Two oscilloscope channel probes are attached to the pair A jumpers for return loss measurement.

For the calibrations for short, open, and load, use the same type of Ethernet cable (straight or crossover) for measurement of the DUT transmitter return loss. For each calibration, connect the Ethernet port on the Differential Return Loss portion to the corresponding Ethernet port on the calibration board attachment for the compliance test board. Once the calibrations are applied, run the test with the DUT. Pass specification is based on the return loss remaining under the mask.

FIGURE 11: 10BASE-T TRANSMITTER RETURN LOSS

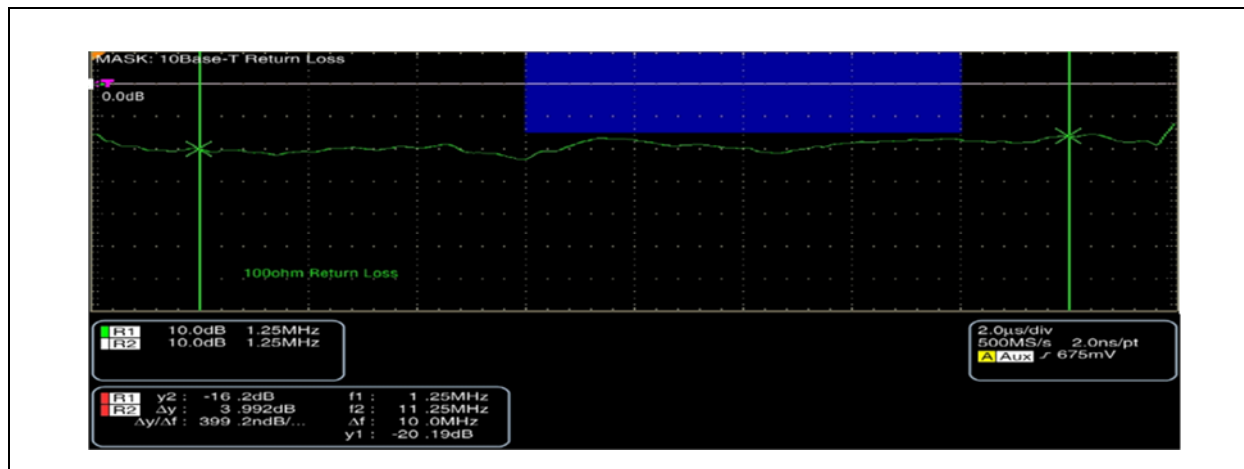


Receiver Return Loss

This is a test of the receiver return loss. A differential signal (positive and negative) must be provided externally from a waveform generator to the test board. The differential signal is fed back to the oscilloscope running the return loss measurements. Two oscilloscope channel probes are attached to the pair B jumpers for return loss measurement.

For the calibrations for short, open, and load, use the same type of Ethernet cable (straight or crossover) for measurement of the DUT receiver return loss. For each calibration, connect the Ethernet port on the Differential Return Loss portion to the corresponding Ethernet port on the calibration board attachment for the compliance test board. Once the calibrations are applied, run the test with the DUT. Pass specification is based on the return loss remaining under the mask.

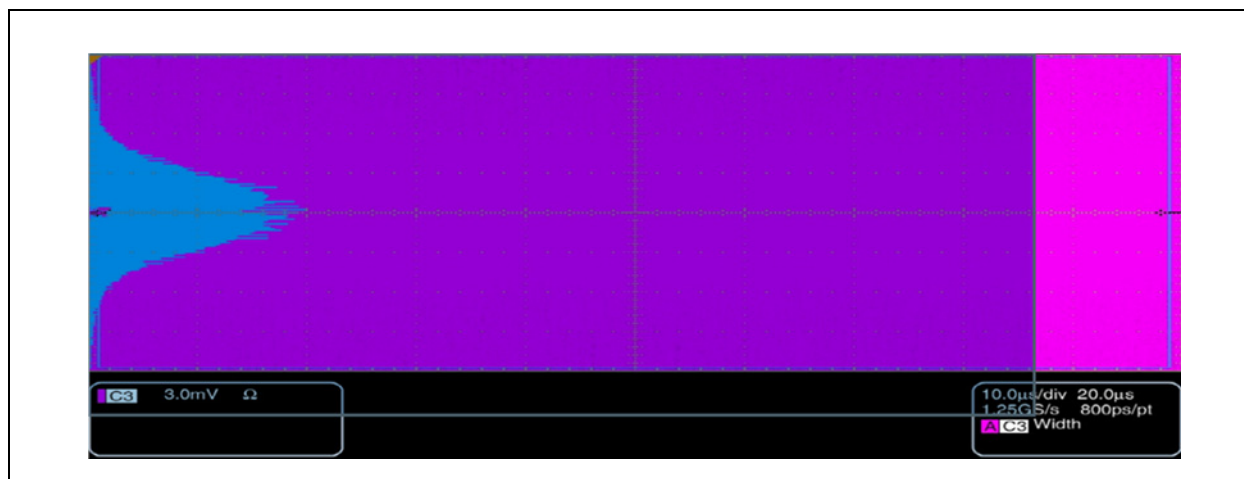
FIGURE 12: 10BASE-T RECEIVER RETURN LOSS



Common-Mode Voltage

This is a test of the common-mode voltage of the 10BASE-T signal. The DUT is connected to the DUT port for the Common-Mode Output Voltage Test, and the oscilloscope cable is connected to the test cable port. Use a jumper to short the differential pair A. To configure the DUT for common-mode voltage testing, refer to [10BASE-T Loopback Mode on KSZ parts](#) register settings. For LAN78xx, refer to the [10BASE-T Pseudo-Random Signal Setting – LAN78xx](#) for register settings. Pass specification is based on common-mode voltage less than 50 mV.

FIGURE 13: 10BASE-T COMMON-MODE VOLTAGE



10BASE-T Compliance Test Signal Generation

Note: W 00 0100h is a write to PHY register 00 of value 0100 in hexadecimal.

For 10BASE-T compliance test on any part, the link pulse and auto-MDIX can be set with the following:

10BASE-T Link Pulse Setting on any part

```
W    00    0100h    // Sets link to 10 Mbps without auto-negotiation
```

For KSZxxxx parts, the rest of the testing is done by enabling the remote loopback, forcing MDI mode, and disabling Auto-MDIX.

10BASE-T Loopback Mode on KSZ parts

For KSZ9xxx PHYs and KSZ Switches:

```
W    00    0100h    // Sets link to 10 Mbps - Full Duplex, Disables Auto-Negotiation
W    11    bit[8] = 1 // Enables remote loopback
W    1C    00C0      // Forces MDI mode and disables Auto-MDIX
```

For KSZ8xxx PHYs:

```
W    00    0100h    // Sets link to 10 Mbps - Full Duplex, Disables Auto-Negotiation
W    1F    A000      // Forces MDI mode and disables Auto-MDIX
```

For LANxxxx parts other than LAN78xx, the rest of the testing is done by enabling loopback mode, forcing MDI mode, and disabling Auto-MDIX. The following enables loopback:

10BASE-T Loopback Mode on LAN parts (except LAN78xx)

```
W    00    4100h    // Enables Loopback, Sets link to 10 Mbps - Full Duplex, Disables
                    Auto-Negotiation
W    11    A000h    // Forces MDI mode and disables Auto-MDIX (Note: Write 0020h for
                    LAN7500)
```

For LAN78xx, a packet generator is available to generate the pseudo-random and all ones signals for the remainder of the 10BASE-T compliance testing. The following enables these modes:

10BASE-T Pseudo-Random Signal Setting – LAN78xx

```
W    12    0020h    // Disables Auto-MDIX
W    00    0100h    // Sets link to 10 Mbps without auto-negotiation
W    1f    0001h    // Sets to Ethernet Page 1 Access
W    13    0008h    // Force MDI mode
W    1d    33FEh    // Resets the packet generation
W    1d    F3FEh    // Sets link to send packets continuously, the destination MAC and
                    source MAC to set to FF:FF:FF:FF:FF:FF (broadcast), random pay-
                    load data with good CRCs
```

10BASE-T All Ones Signal for Harmonic Distortion – LAN78xx

```
W    12    0020h    // Disables Auto-MDIX
W    00    0100h    // Sets link to 10 Mbps without auto-negotiation
W    1f    0001h    // Sets to Ethernet Page 1 Access
W    13    0008h    // Force MDI mode
W    1e    FFFFh    // Sets packet generator to send FFFF each 16 bits of payload data,
                    which is all ones
W    1d    33FCh    // Resets the packet generation payload to the new payload pattern
                    written to the ECG register in the previous step
W    1d    F3FCh    // Sets link to send packets continuously, the destination MAC and
                    source MAC to set to FF:FF:FF:FF:FF:FF (broadcast), fixed payload
                    data with good CRCs
```

100BASE-TX COMPLIANCE TESTING

The 100BASE-TX compliance tests are:

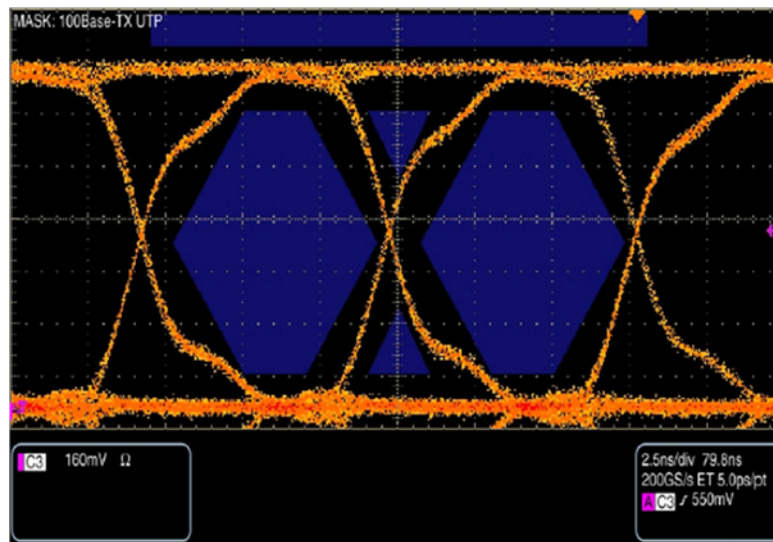
- Template
- Differential Output Voltage
- Signal Amplitude Symmetry
- Rise Time
- Fall Time
- Rise Time/Fall Time Symmetry
- Waveform Overshoot
- Transmit Jitter
- Distortion Based on Duty Cycle
- Transmitter Return Loss
- Receiver Return Loss

All tests use transmit scrambled idles for 100BASE-TX. Refer to [100BASE-TX Setting – Transmit Scrambled Idles](#) for the register settings.

Template

This is a test of the voltage points on the 100BASE-TX Ethernet signal. The DUT is connected to the Ethernet port for the Loads and Probes Test, and the oscilloscope cable is connected to the TX test jumper (Pair A). Pass specification is the signal that must be within the mask.

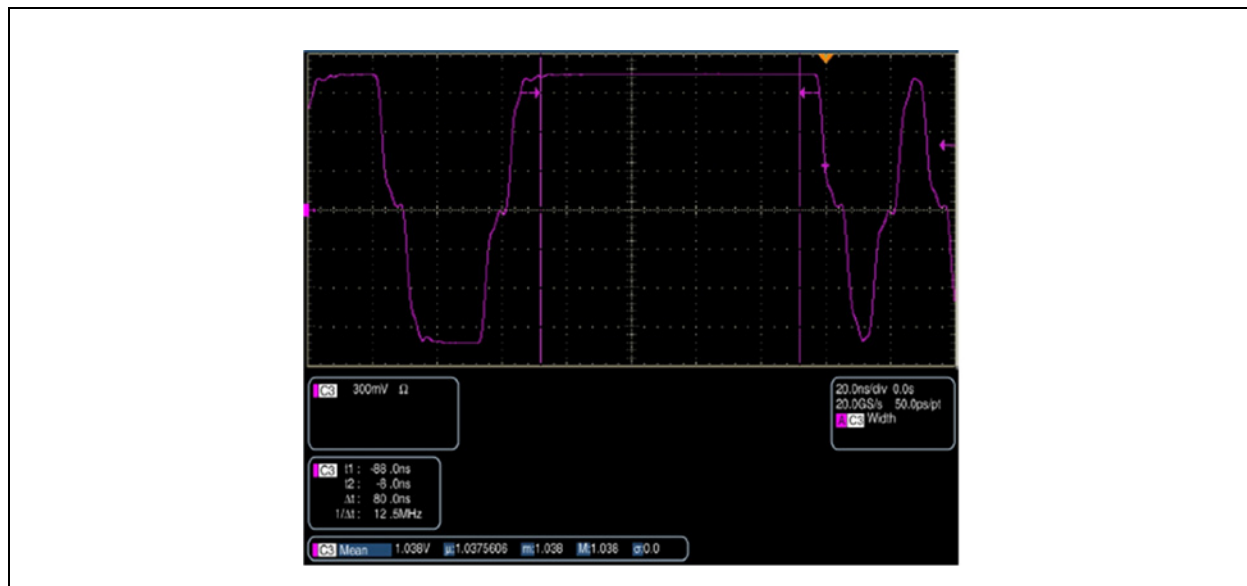
FIGURE 14: 100BASE-TX TEMPLATE



Differential Output Voltage

This is a test of the differential voltage 100BASE-TX Ethernet signal. The DUT is connected to the Ethernet port for the Loads and Probes Test, and the oscilloscope cable is connected to the TX test jumper (Pair A). Pass specification is based on $+V_{out}$ between 950 mV and 1050 mV, and on $-V_{out}$ between -1050 mV and -950 mV.

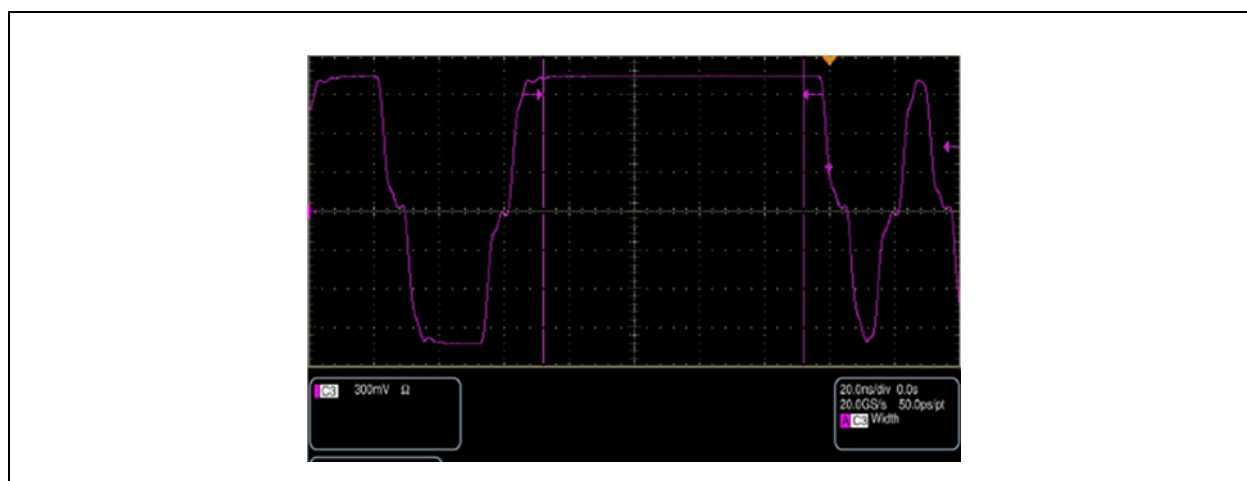
FIGURE 15: 100BASE-TX DIFFERENTIAL OUTPUT VOLTAGE



Signal Amplitude Symmetry

This is a test of the 100BASE-TX Ethernet signal amplitude symmetry. The DUT is connected to the Ethernet port for the Loads and Probes Test, and the oscilloscope cable is connected to the TX test jumper (Pair A). Pass specification is 0.98 to 1.02.

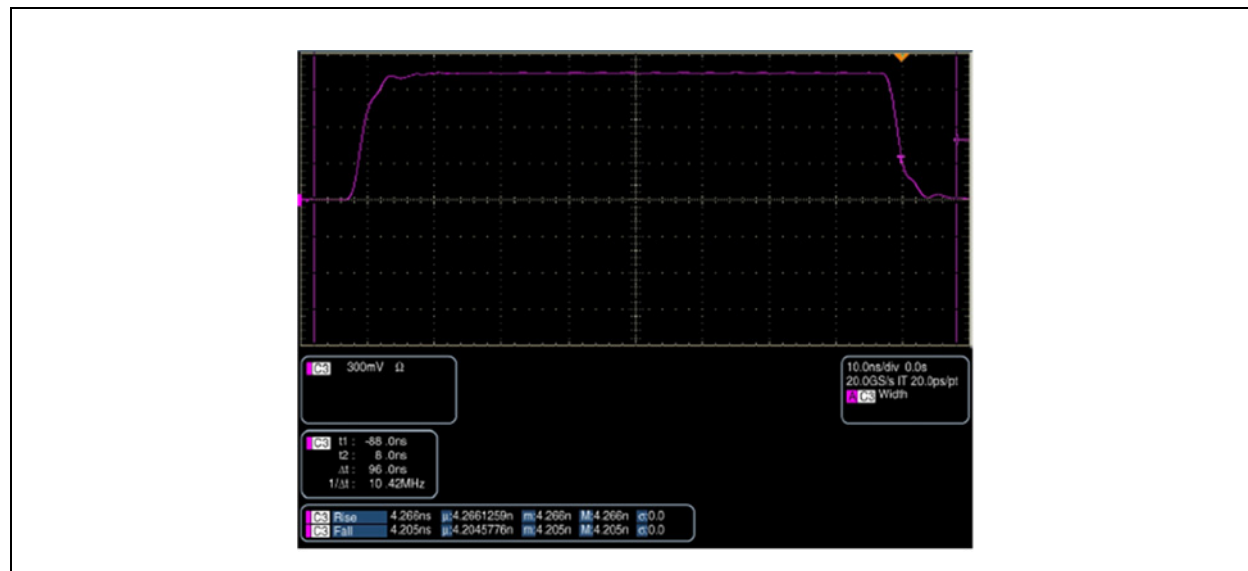
FIGURE 16: 100BASE-TX SIGNAL AMPLITUDE SYMMETRY



Rise Time

This is a test of the rise time of the 100BASE-TX Ethernet differential signals. The DUT is connected to the Ethernet port for the Loads and Probes Test, and the oscilloscope cable is connected to the TX test jumper (Pair A). Pass specification is 3 ns to 5 ns on both positive and negative differential signals.

FIGURE 17: 100BASE-TX RISE TIME-FALL TIME AND RISE/FALL SYMMETRY



Fall Time

This is a test of the fall time of the 100BASE-TX Ethernet differential signals. The DUT is connected to the Ethernet port for the Loads and Probes Test, and the oscilloscope cable is connected to the TX test jumper (Pair A). Pass specification is 3 ns to 5 ns on both positive and negative differential signals.

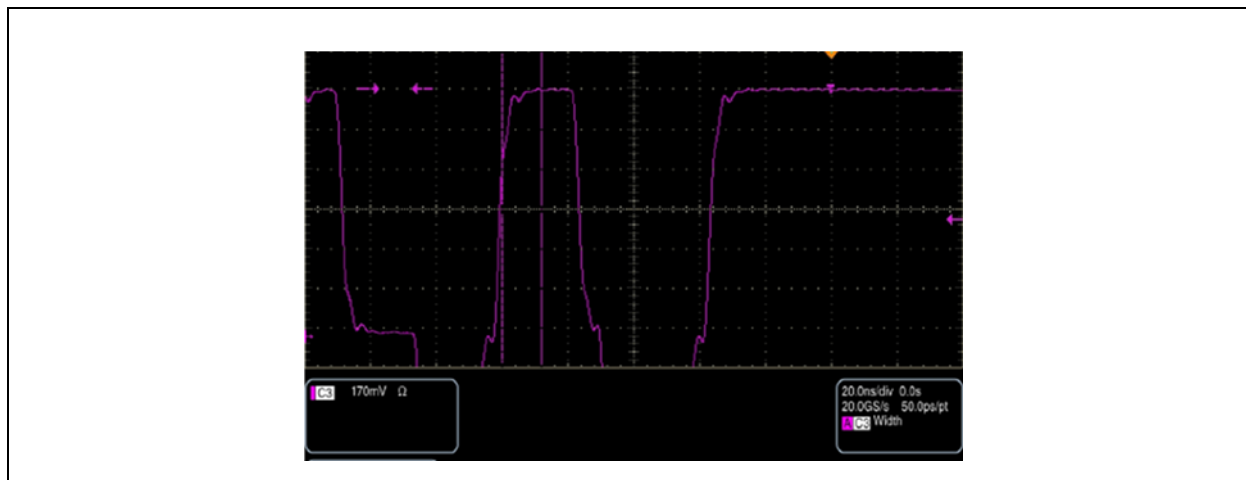
Rise Time/Fall Time Symmetry

This is a test of the symmetry of the rise and fall times on the 100BASE-TX Ethernet differential signals. The DUT is connected to the Ethernet port for the Loads and Probes Test, and the oscilloscope cable is connected to the TX test jumper (Pair A). Pass specification is less than 500 ps on both positive and negative differential signals.

Waveform Overshoot

This is a test of the overshoot of the 100BASE-TX Ethernet signal. The DUT is connected to the Ethernet port for the Loads and Probes Test, and the oscilloscope cable is connected to the TX test jumper (Pair A). Pass specification is less than 5% overshoot on both positive and negative differential signals.

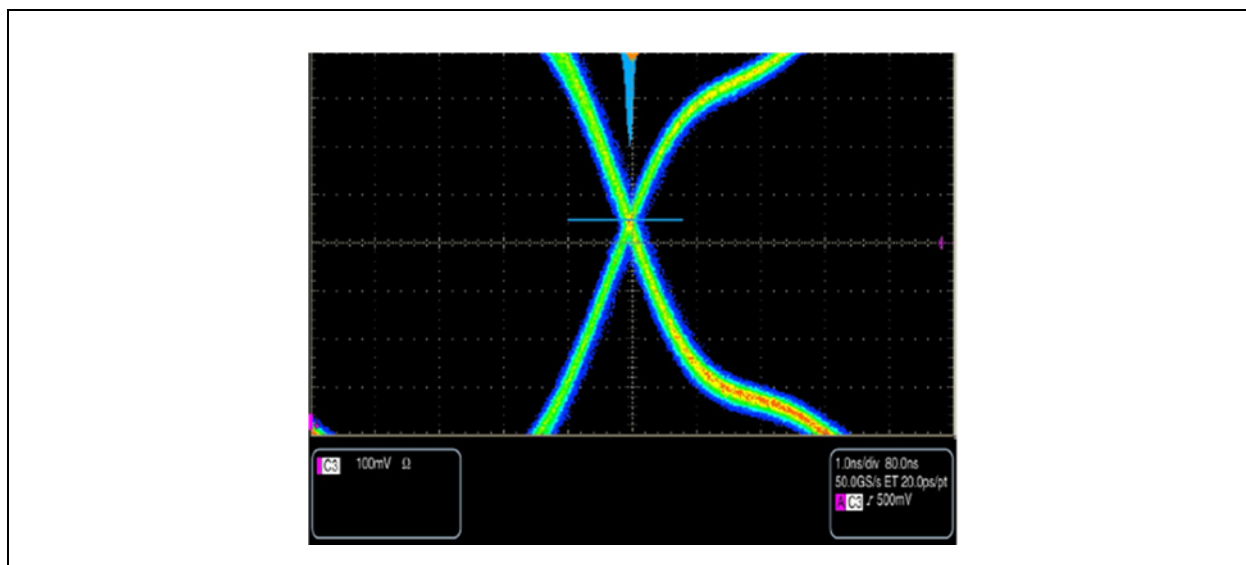
FIGURE 18: 100BASE-TX WAVEFORM OVERSHOOT



Transmit Jitter

This is a test of the jitter on the 100BASE-TX Ethernet signal. The DUT is connected to the Ethernet port for the Loads and Probes Test, and the oscilloscope cable is connected to the TX test jumper (Pair A). Pass specification is less than 1.4 ns of the jitter.

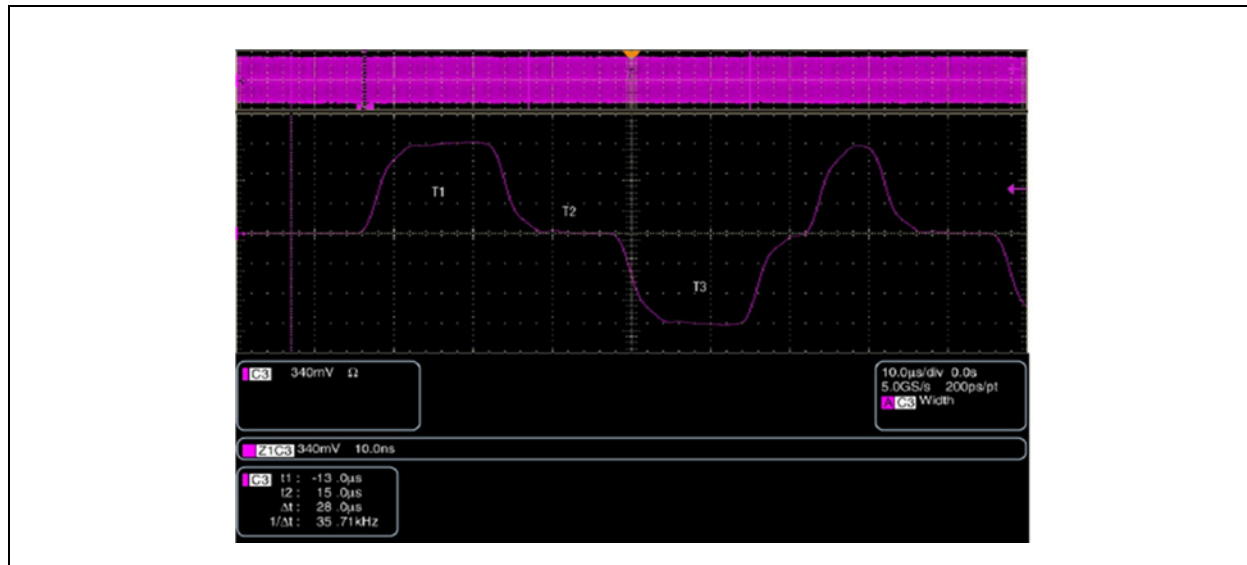
FIGURE 19: 100BASE-TX TRANSMIT JITTER



Distortion Based on Duty Cycle

This is a test of the distortion based on the duty cycle of the 100BASE-TX Ethernet signal. The DUT is connected to the Ethernet port for the Loads and Probes Test, and the oscilloscope cable is connected to the TX test jumper (Pair A). Pass specification is distortion is less than 500 ps.

FIGURE 20: 100BASE-TX DISTORTION - DUTY CYCLE

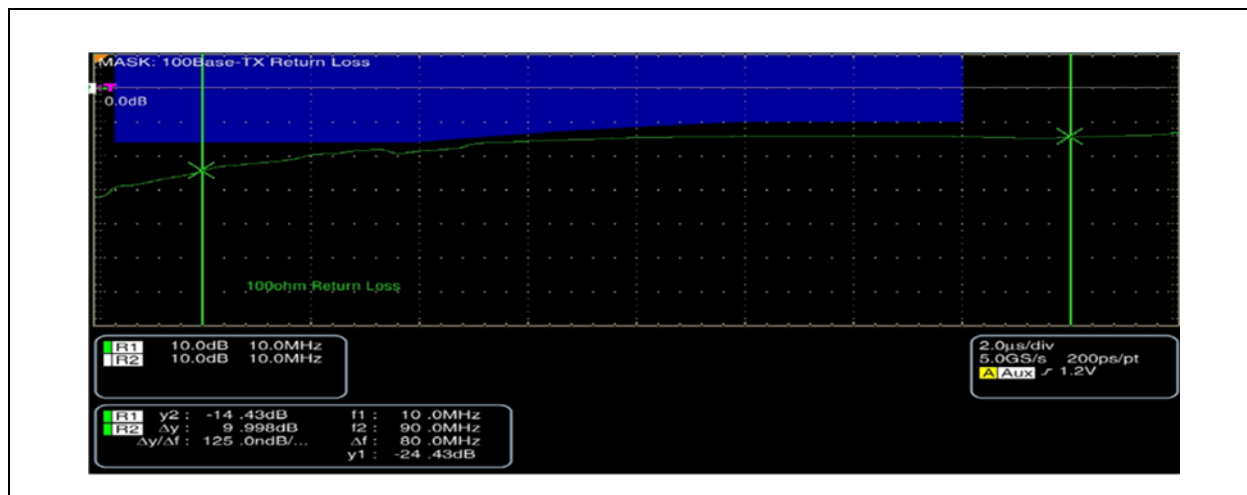


Transmitter Return Loss

This is a test of the transmitter return loss. A differential signal (positive and negative) must be provided externally from a waveform generator to the test board. The differential signal is fed back to the oscilloscope running the return loss measurements. Two oscilloscope channel probes are attached to the pair A jumpers for return loss measurement.

For the calibrations for short, open, and load, use the same type of Ethernet cable (straight or crossover) for measurement of the DUT transmitter return loss. For each calibration, connect the Ethernet port on the Differential Return Loss portion to the corresponding Ethernet port on the calibration board attachment for the compliance test board. Once the calibrations are applied, run the test with the DUT. Pass specification is based on the return loss remaining under the mask.

FIGURE 21: 100BASE-TX TRANSMITTER RETURN LOSS

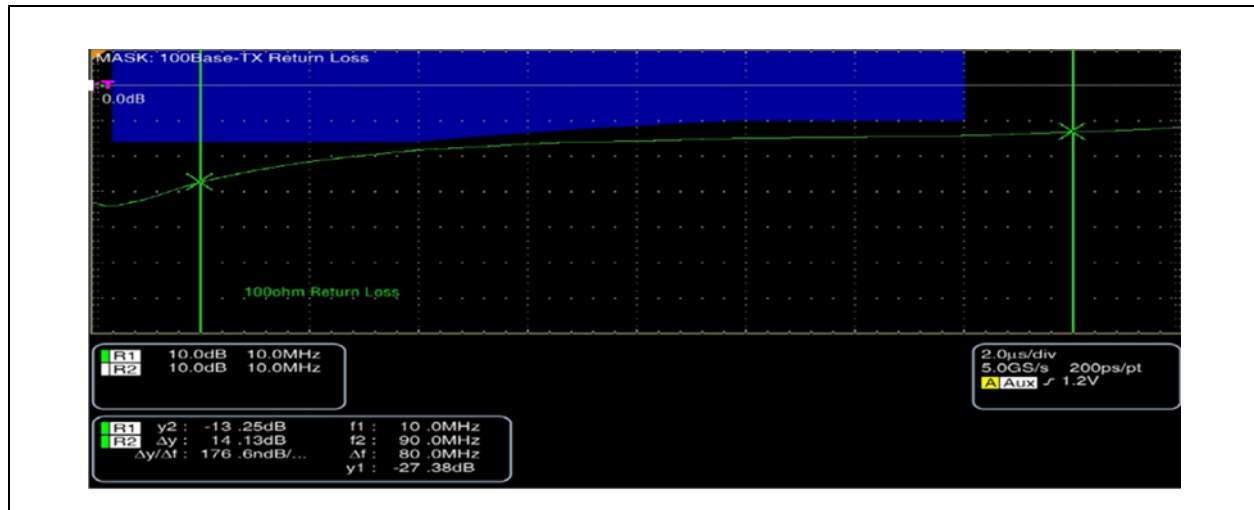


Receiver Return Loss

This is a test of the receiver return loss. A differential signal (positive and negative) must be provided externally from a waveform generator to the test board. The differential signal is fed back to the oscilloscope running the return loss measurements. Two oscilloscope channel probes are attached to the pair B jumpers for return loss measurement.

For the calibrations for short, open, and load, use the same type of Ethernet cable (straight or crossover) for measurement of the DUT receiver return loss. For each calibration, connect the Ethernet port on the Differential Return Loss portion to the corresponding Ethernet port on the calibration board attachment for the compliance test board. Once the calibrations are applied, run the test with the DUT. Pass specification is based on the return loss remaining under the mask.

FIGURE 22: 100BASE-TX RECEIVER RETURN LOSS



100BASE-TX Compliance Test Signal Generation

Note: W 00 2100h is a write to PHY register 00 of value 2100 in hexadecimal.

100BASE-TX Setting – Transmit Scrambled Idles

For KSZ9xxx PHYs and KSZ Switches:

```
W 00 2100h // Sets link to 100 Mbps - Full Duplex, Disable Auto-Negotiation
W 1C 00C0h // Forces MDI mode and disables Auto-MDIX
```

For KSZ8xxx PHYs:

```
W 00 2100h // Sets link to 100 Mbps - Full Duplex, Disable Auto-Negotiation
W 1F A000h // Forces MDI mode and disables Auto-MDIX
```

For LAN parts (except LAN78xx):

```
W 00 2100h // Sets link to 100 Mbps - Full Duplex, Disable Auto-Negotiation
W 11 A000h // Forces MDI mode and disables Auto-MDIX (Note: Write 0020h for LAN7500)
```

For LAN78xx:

```
W 12 0020h // Disables Auto-MDIX
W 00 2100h // Sets link to 100 Mbps - Full Duplex, Disable Auto-Negotiation
W 1f 0001h // Sets to Ethernet Page 1 Access
W 13 0008h // Force MDI Mode
```

1000BASE-T COMPLIANCE TESTING

The 1000BASE-T compliance tests are:

- Peak Differential Output Voltage
- Output Droop
- Template
- Jitter – Master
- Jitter – Slave
- Transmitter Distortion
- Common-Mode Voltage
- Return Loss

Each test must be done for all four Ethernet twisted pairs. The test mode waveforms are found in the Test Mode Tutorial page of the UNH IOL website, along with all of the points used for Peak Differential Output, Output Droop, and Template testing.

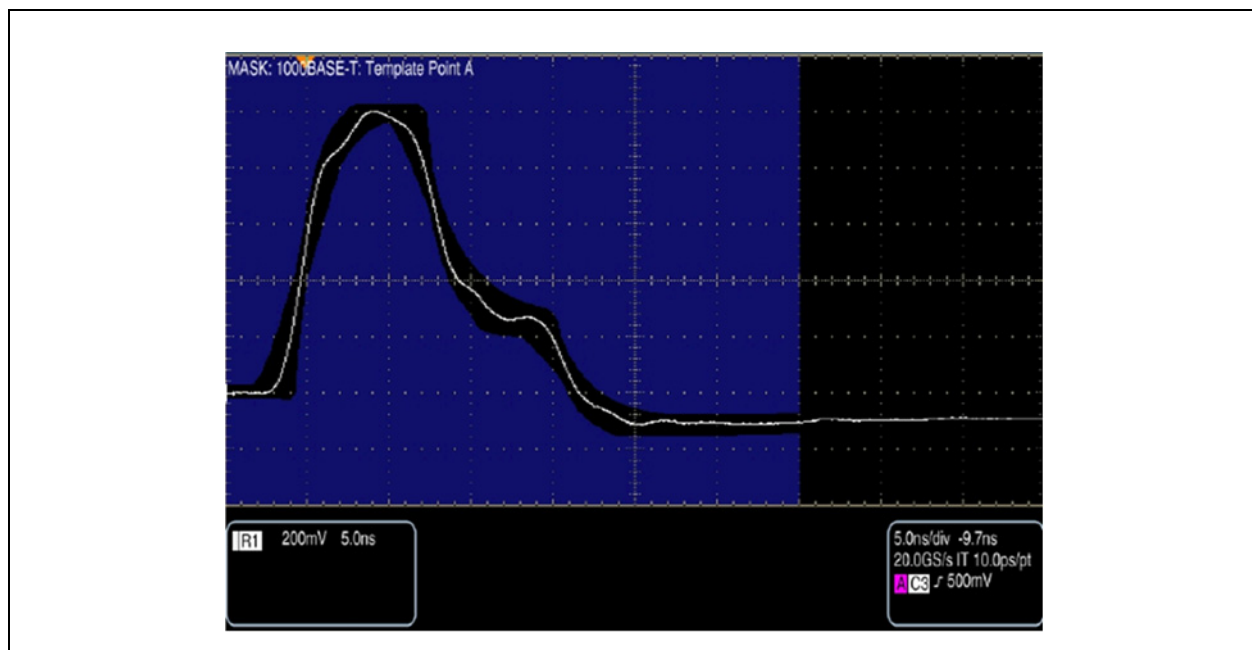
Peak Differential Output Voltage

This is a test of the peak differential output voltage of the 1000BASE-T signal. The DUT is connected to the Ethernet port for the Loads and Probes Test, and the oscilloscope cable is connected to the probe differential pair under test. To configure the DUT for Peak Differential Output Voltage testing, refer to the [1000BASE-T Compliance Testing - Test Mode 1 Waveform](#) register settings.

Pass specification is based on the following:

- Peak differential output voltage is between 670 mV and 820 mV for points A and B.
- The magnitude difference between points A and B is less than 1%.
- The magnitude difference of point C from 0.5 multiplied by the average magnitudes of points A and B is less than 2%.
- The magnitude difference of point D from 0.5 multiplied by the average magnitudes of points A and B is less than 2%.

FIGURE 23: 1000BASE-T PEAK DIFFERENTIAL VOLTAGE



Output Droop

This is a test of the output droop of the 1000BASE-T signal. The DUT is connected to the Ethernet port for the Loads and Probes Test, and the oscilloscope cable is connected to the probe differential pair under test. To configure the DUT for Output Droop testing, refer to the [1000BASE-T Compliance Testing - Test Mode 1 Waveform](#) register settings.

Pass specification is based on the following:

- The magnitude at point G is greater than 73.1% the magnitude at point F.
- The magnitude at point J is greater than 73.1% the magnitude at point H.

FIGURE 24: 1000BASE-T OUTPUT DROOP - POINT G

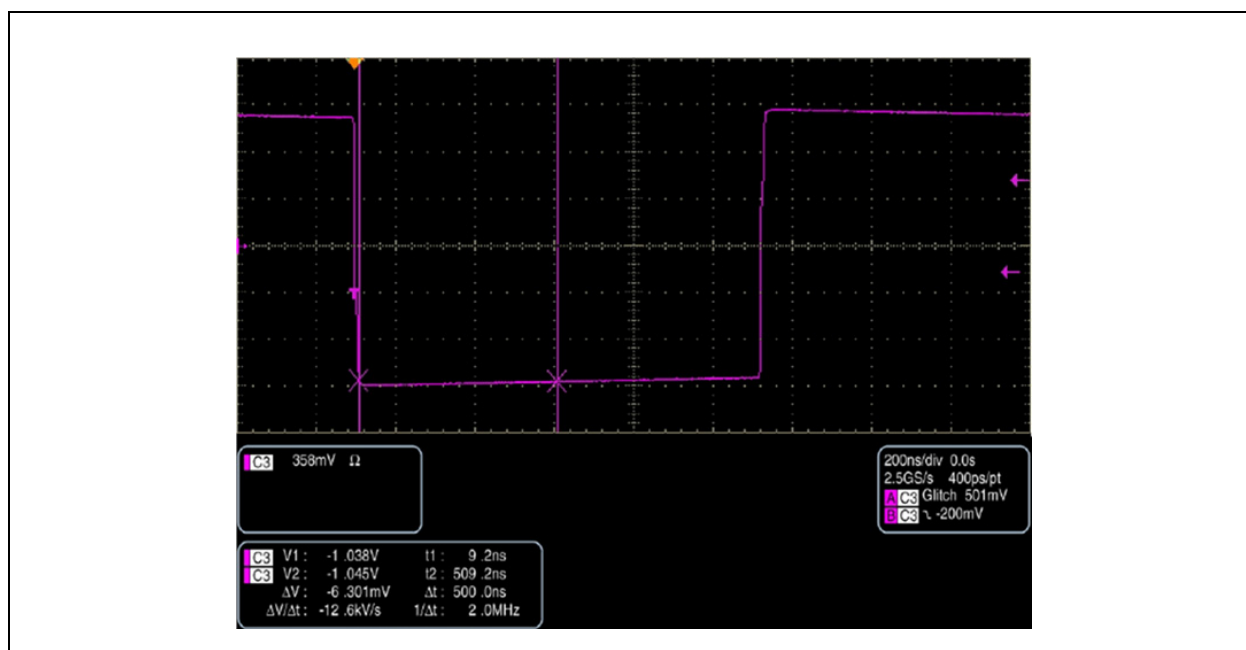
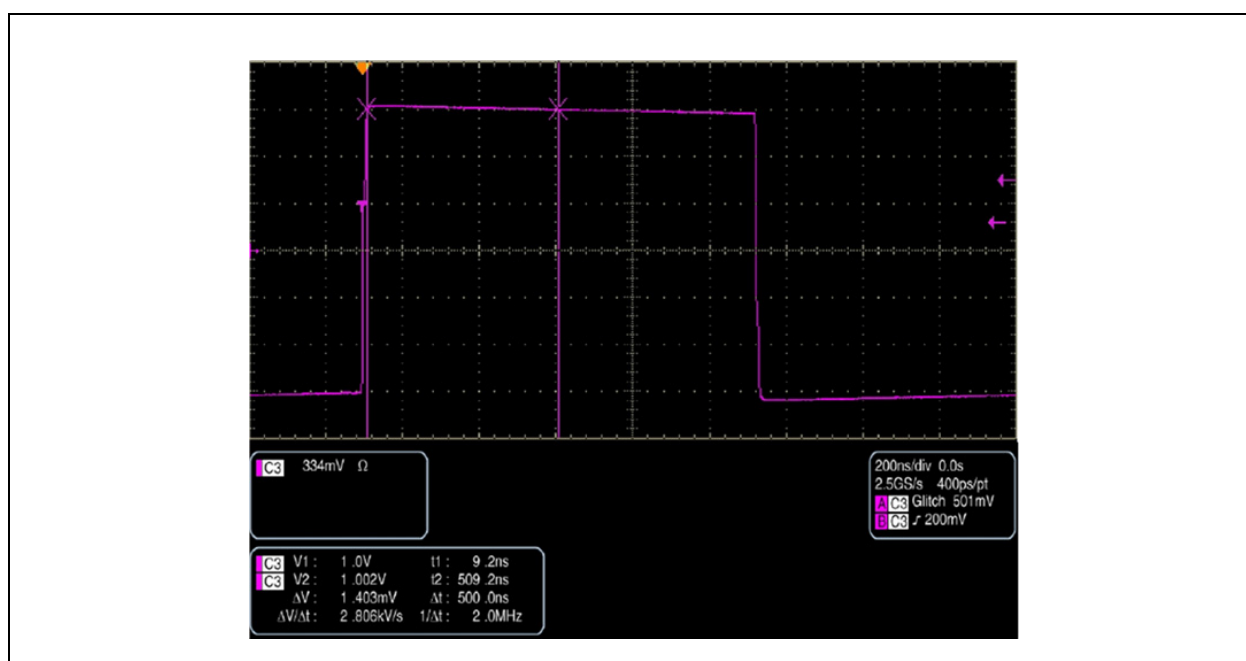


FIGURE 25: 1000BASE-T OUTPUT DROOP - POINT J



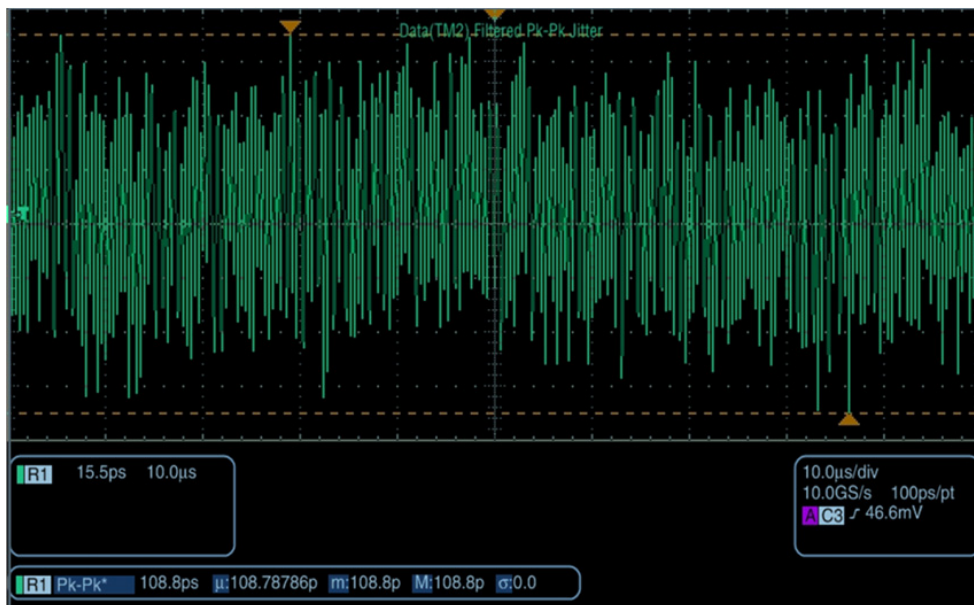
Template Tests

This is a test of the voltage points for the test mode 1 1000BASE-T waveform using templates for each voltage point. The DUT is connected to the Ethernet port for the Loads and Probes Test, and the oscilloscope cable is connected to the probe differential pair under test. To configure the DUT for 1000BASE-T Template testing, refer to the [1000BASE-T Compliance Testing - Test Mode 1 Waveform](#) register settings. Pass specification is for all templates to fall within the mask allowed for voltage points A, B, C, D, F, and H. See [Figure 23](#) for reference.

Jitter - Master

This is a test of the jitter when the DUT is the master. The DUT is connected to the Ethernet port for the Loads and Probes Test, and the oscilloscope cable is connected to the probe differential pair under test. To configure the DUT for the test, refer to the [1000BASE-T Jitter Testing as Master – Test Mode 2 Waveform](#) register settings. The test runs an unfiltered jitter test and a filtered jitter test through a 5-kHz high-pass filter. Pass specification is for unfiltered jitter less than 1.4 ns and for filtered jitter less than 0.3 ns.

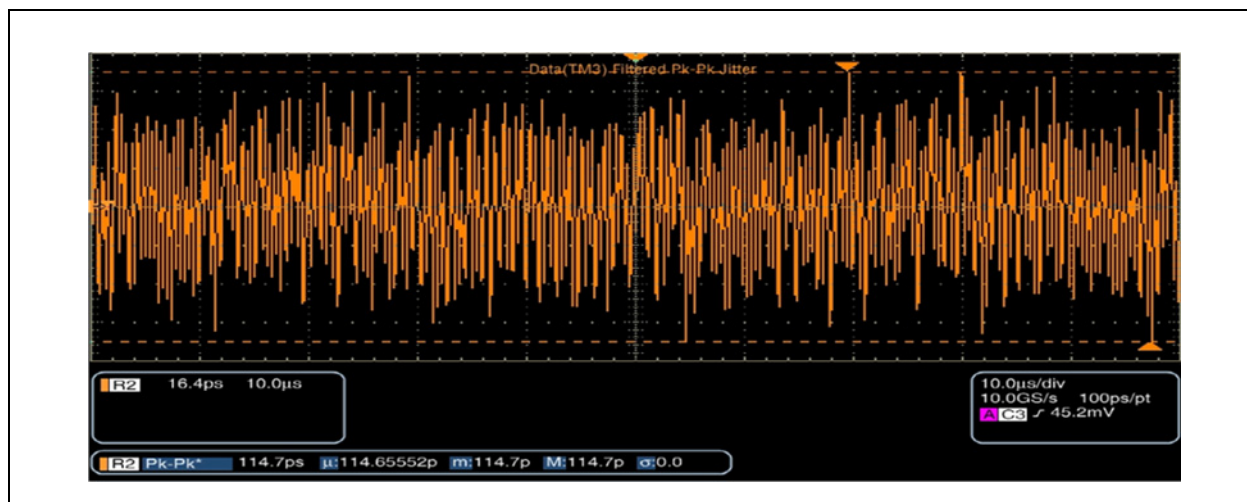
FIGURE 26: 1000BASE-T MASTER JITTER FILTERED



Jitter - Slave

This is a test of the jitter when the DUT is the slave. The DUT is connected to the Ethernet port for the Loads and Probes Test, and the oscilloscope cable is connected to the probe differential pair under test. To configure the DUT for the test, refer to the [1000BASE-T Jitter Testing as Master – Test Mode 2 Waveform](#) register settings for the first part and to the [1000BASE-T Jitter Testing as Slave – Test Mode 3 Waveform](#) register settings for the second part. The test runs an unfiltered jitter test and a filtered jitter test through a 5-kHz high-pass filter. Pass specification is for unfiltered jitter less than 1.4 ns and for filtered jitter less than 0.4 ns.

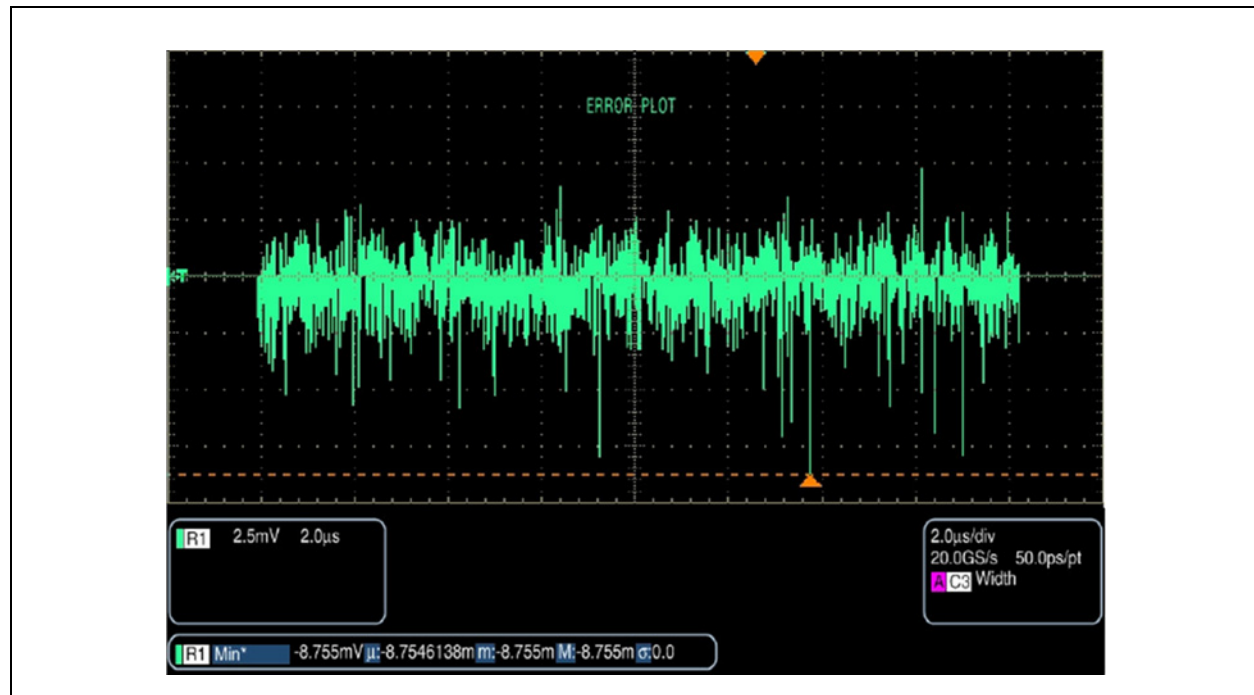
FIGURE 27: 1000BASE-T SLAVE JITTER FILTERED



Transmitter Distortion

This is a test of the Waveform Distortion. The DUT is connected to the Ethernet port for the Loads and Probes Test, and the oscilloscope cable is connected to the probe differential pair under test. To configure the DUT for the test, refer to the [1000BASE-T Compliance Testing – Test Mode 4 Waveform](#) register settings. Pass specification is distortion less than 10 mV for at least 60% of the unit interval of the eye diagram.

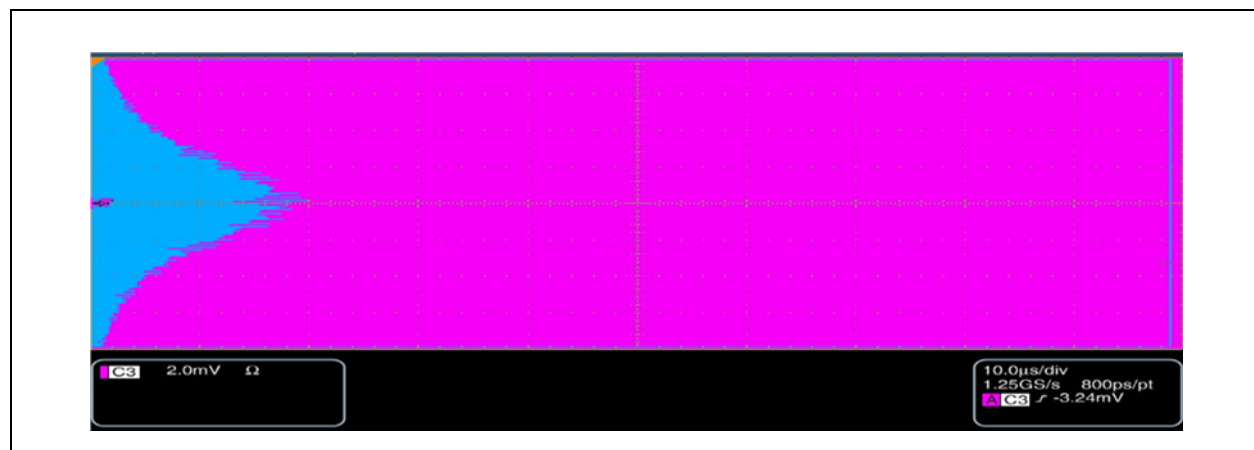
FIGURE 28: 1000BASE-T TRANSMITTER DISTORTION



Common-Mode Output Voltage

This is a test of the common-mode voltage of the waveform. The DUT is connected to the Ethernet port for the Common Mode Output Voltage Test, and the oscilloscope cable is connected to the probe differential pair under test. To configure the DUT for the test, refer to the [1000BASE-T Compliance Testing – Test Mode 4 Waveform](#) register settings. To pass this test, the common-mode output voltage must be less than 50 mV peak-to-peak.

FIGURE 29: 1000BASE-T COMMON-MODE OUTPUT VOLTAGE

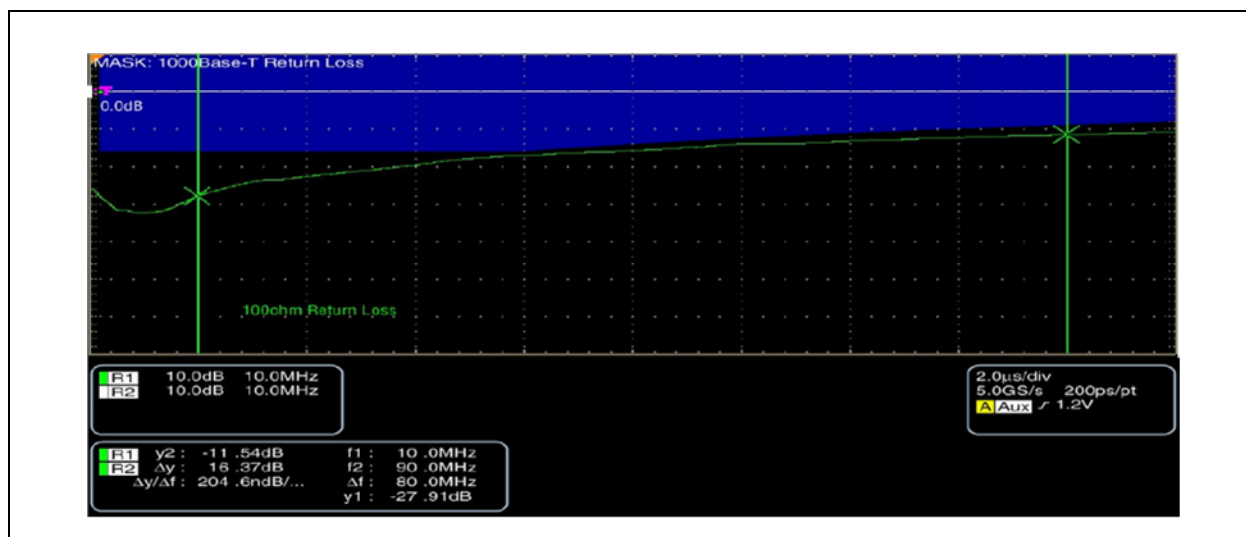


Return Loss

This is a test of the return loss over each differential pair. A differential signal (positive and negative) must be provided externally from a waveform generator to the test board. The differential signal is fed back to the oscilloscope running the return loss measurements. Two oscilloscope channel probes are attached to the differential pair using test jumpers for return loss measurement.

For the calibrations for short, open, and load, use the same type of Ethernet cable (straight or crossover) for measurement of the DUT transmitter return loss. For each calibration, connect the Ethernet port on the Differential Return Loss portion to the corresponding Ethernet port on the calibration board attachment for the compliance test board. Once the calibrations are applied, run the test with the DUT. Pass specification is based on the return loss remaining under the mask.

FIGURE 30: 1000BASE-T RETURN LOSS



1000BASE-T Compliance Test Signal Generation

Note: W 09 3b00h is a write to PHY register 09 of value 3b00 in hexadecimal.

1000BASE-T Compliance Testing - Test Mode 1 Waveform

```
W    00      0140h      // Force 1000 Mbps - Full Duplex, Disable Auto-Negotiation
W    09      3b00h      // Test Mode 1 - Transmit Waveform Test
```

1000BASE-T Jitter Testing as Master – Test Mode 2 Waveform

```
W    00      0140h      // Force 1000 Mbps - Full Duplex, Disable Auto-Negotiation
W    09      5b00h      // Test Mode 2 - Transmit Jitter Test in Master mode
```

1000BASE-T Jitter Testing as Slave – Test Mode 3 Waveform

```
W    00      0140h      // Force 1000 Mbps - Full Duplex, Disable Auto-Negotiation
W    09      7300h      // Test Mode 3 - Transmit Jitter Test in Slave mode
```

1000BASE-T Compliance Testing – Test Mode 4 Waveform

```
W    00      0140h      // Force 1000 Mbps - Full Duplex, Disable Auto-Negotiation
W    09      9b00h      // Test Mode 4 - Transmitter Distortion Test
```

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002686A (04-10-18)	Initial release	

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